## JVC

## SERVICE MANUAL CD RECEIVER

## KD-SH909R



MP3
CD-RiV
PLAYBACK


## Contents

Safety precaution -.......................... 1-2

Flow of functional

Preventing static electricity .-...........-1-3
Disassembly method
1-4
Adjustment method .-....................... 1-23
operation unit TOC read ........... 1-24
Maintenance of laser pickup ..... 1-26
Replacement of laser pickup ..... 1-26
Description of major ICs ..... 1-27~51

## Safety precaution

$\lfloor$ CAUTION Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.
$\lfloor$ CAUTION Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.

## Preventing static electricity

## 1.Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

## 2.About the earth processing for the destruction prevention by static electricity

Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as CD players. Be careful to use proper grounding in the area where repairs are being performed.

## 2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

## 2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.


## 3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

## 4.Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
3. Handle the flexible cable carefully as it may break when subjected to strong force.
4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

## Attention when traverse unit is decomposed

*Please refer to "Disassembly method" in the text for pick-up and how to detach the substrate.
1.Solder is put up before the card wire is removed from connector on the CD substrate as shown in Figure.
(When the wire is removed without putting up solder, the CD pick-up assembly might destroy.)
2.Please remove solder after connecting the card wire with when you install picking up in the substrate.


## Disassembly method

## - Removing the front panel assembly

(See Fig.1)

1. Press the release button in the lower right part of the front panel assembly to unlock.
2. Remove the front panel assembly in the direction of the arrow.

## ■Removing the top chassis

(See Fig. 2 to 6)

- Turn on power.

1. Press the eject button in the upper left part of the front panel assembly to move the assembly as shown in Fig. 2 and turn off power.
2. Remove the two screws $\mathbf{A}$ on the upper side of the body.


Fig. 1


Fig. 2


Fig. 3
3. Remove the three screws $\mathbf{B}$ on both sides of the body.
4. Remove the screw $\mathbf{C}$ and the three screws $\mathbf{D}$ on the left side of the body.
5. Remove the two screws $\mathbf{E}$ and the screw $\mathbf{F}$ on the back of the body.
6. Move the top chassis upward and remove it with the CD mechanism assembly. The connector on the CD mechanism assembly is disconnected from connector CN601 on the main board.


Fig. 5


Fig. 6

## ■Removing the (A) board

(See Fig.7)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the wire from connector CN601on the (A) board.
2. Remove the five screws $\mathbf{G}$ and the (A) board, releasing the joint $\mathbf{a}$ and $\mathbf{b}$.


Fig. 4


Fig. 7

## Removing the CD mechanism assembly (See Fig.8)

- Prior to performing the following procedure, remove the top chassis.

1. Remove the three screws $\mathbf{H}$ inside the top chassis and remove the CD mechanisma ssembly.

## ■Removing the motor assembly

(See Fig. 9 to 11)

- Prior to performing the following procedure, remove the top chassis.

1. Disconnect the wire from connector CN703 on the main board.
2. Remove the motor bracket and the spring attached to the arm braket assembly (R).
3. Remove the two screws I attaching the motor bracket.
4. Remove the washer attaching the clutch assembly and pull out the clutch assembly from the shaft.
5. Remove the two screws $\mathbf{J}$ and the motor assembly from the motor bracket.


Fig. 11


Fig. 8


Fig. 9


Fig. 10

## Removing the main board

## (See Fig. 12 to 16)

- Prior to performing the following procedures, remove the top chassis and the motor bracket.

1. Disconnect the flexible wire from connector CN701 and CN702 on the main board respectively.
2. Move the front bracket backward until it stops.
3. Remove the four screws $\mathbf{K}$ attaching the arm brackets (L) and (R). Move the right and arm lefter brackets from the rod gear.
4. Remove the rod gear.
5. Remove the screw $\mathbf{M}$ attaching the rear panel to the bottom cover on the back of the body.


Fig. 12


Fig. 13


Fig. 14
6. Remove the two screws $\mathbf{L}$ and move the main board backwards to release the two joints c. (The main board will be removed with the rear panel and the rear heat sink)
7. Remove the screw $\mathbf{N}$ and $\mathbf{Q}$ attaching the rear heat sink.
8. Remove the three screws $\mathbf{O}$ and the screw $\mathbf{P}$ attaching the rear panel. Remove the main board.


Fig. 15


Fig. 16


Fig. 17

## $\square$ Removing the lifter board

(See Fig. 18 to 24)

- Prior to performing the following procedure, remove the top chassis assembly and thefront panel assembly.

1. Disconnect the flexible wire from connector CN702 on the main board.
2. Remove the four screws $\mathbf{S}$ attaching the front bracket on both sides of the body.
3. Push the pin of the joint $\mathbf{d}$ on the front of the front bracket to release the lock lever.


Fig. 18


Fig. 19

4. Remove the screw $\mathbf{T}$ attaching the lifter board cover in the rear of the front bracket.
5. Release the two joints $\mathbf{f}$ while pushing the front side. Move the lifter board cover inthe direction of the arrow and release the eight joints $\mathbf{e}$.
6. Remove the two screws $\mathbf{U}$ attaching the lifter board on the front of the body.


Fig. 22


Fig. 23


Fig. 24

## <Front panel assembly>

- Prior to performing the following procedure, remove the front panel assembly.

Removing the front board
(See Fig. 25 and 26)

1. Remove the four screws $\mathbf{V}$ attaching the rear panel to the front panel assembly.
2. Release the eleven joints $\mathbf{g}$ of the front panel and the rear panel.
3. Disconnect the wire from connector CN803 on the front board.
4. If necessary, unsolder the front board.

## - Removing the volume board

(See Fig. 26 and 27)

- Prior to performing the following procedure, remove the rear panel.

1. Remove the four screws $\mathbf{W}$ attaching the volume board.
2. Disconnect the volume knob, ring lens and volume ring from the volume board.
3. If necessary, unsolder the volume board.

## - Removing the line in board

(See Fig. 26 and 28)

- Prior to performing the following procedure, remove the rear panel.

1. Disconnect the wire from connector CN803 on the front board.
2. Pull out the line in board from the front panel assembly.


Fig. 25


Fig. 26


Rng knob
Fig. 27


Fig. 28

## < CD mechanism section > $\square$ Removing the top cover

(See Fig. 1 and 2)

1. Remove the two screws $\mathbf{A}$ on each side of the body.
2. Lift the front side of the top cover and move the cover backward to release the two joints a.

## ■Removing the connector board

(See Fig. 3 to 5)
CAUTION: Before disconnecting the flexible wire from the pickup, solder the short-circuit point on the pickup. No observance of this instruction may cause damage of the pickup.

1. Remove the screw $\mathbf{B}$ fixing the connector board.
2. Solder the short-circuit point on the connector board.

Disconnect the flexible wire from the pickup.
3. Move the connector board in the direction of the arrow to release the two joints $\mathbf{b}$.
4. Unsolder the wire on the connector board if necessary.

CAUTION: Unsolder the short-circuit point after reassembling.


Fig. 1


Fig. 2


Fig. 3


Fig. 4

Fig. 5

## - Removing the DET switch

## (See Fig. 3 and 6)

1. Extend the two tabs $\mathbf{c}$ of the feed sw. holder and pull out the switch.
2. Unsolder the DET switch wire if necessary.

## Removing the chassis unit

## (See Fig. 7 and 8)

- Prior to performing the following procedure, remove the top cover and the connector board.


Fig. 3

1. Remove the two suspension springs (L) and (R) attaching the chassis unit to the frame.

CAUTION: The shape of the suspension spring (L) and $(R)$ are different. Handle them with care.

CAUTION: When reassembling, make sure that the three shafts on the underside of the chassis unit are inserted to the dampers certainly.


Fig. 6


Fig. 7
Fig. 8

## ■Removing the clamper assembly

 (See Fig. 9 and 10)- Prior to performing the following procedure, remove the top cover.

1. Remove the clamper arm spring.
2. Move the clamper assembly in the direction of the arrow to release the two joints $\mathbf{d}$.

## ■Removing the loading / feed motor assembly (See Fig. 11 and 12)

- Prior to performing the following procedure, remove the top cover, the connector board and the chassis unit.

1. Remove the screw $\mathbf{C}$ and move the loading / feed motor assembly in the direction of the arrow to remove it from the chassis rivet assembly.
2. Disconnect the wire from the loading / feed motor assembly if necessary.

CAUTION: When reassembling, connect the wire from the loading / feed motor assembly to the flame as shown in Fig. 11.


Loading / feed motor assembly
Fig. 11

Fig. 10


Fig. 9


Fig. 12

## Removing the pickup unit

(See Fig. 13 to 17)

- Prior to performing the following procedure, remove the top cover, the connector board and the chassis unit.

1. Remove the screw $\mathbf{D}$ and pull out the pu. shaft holder from the shaft.
2. Remove the screw $\mathbf{E}$ attaching the feed sw. holder.
3. Move the part $\mathbf{e}$ of the pickup unit upward with the shaft and the feed sw. holder, then release the joint $f$ of the feed sw. holder in the direction of the arrow. The joint $\mathbf{g}$ of the pickup unit and the feed rack is released, and the feed sw. holder comes off.
4. Remove the shaft from the pickup unit.
5. Remove the screw $\mathbf{F}$ attaching the feed rack to the pickup unit.

## $\square$ Reattaching the pickup unit

(See Fig. 13 to 16)

1. Reattach the feed rack to the pickup unit using the screw F.
2. Reattach the feed sw. holder to the feed rack while setting the joint tab $\mathbf{g}$ to the slot of the feed rack and setting the part f of the feed rack to the switch of the feed sw. holder correctly.
3. As the feed sw. holder is temporarily attached to the pickup unit, set to the gear of the joint $\mathbf{g}$ and to the bending part of the chassis (joint $\mathbf{h}$ ) at a time.

CAUTION: Make sure that the part $i$ on the underside of the feed rack is certainly inserted to the slot $\mathbf{j}$ of the change lock lever.
4. Reattach the feed sw. holder using the screw $\mathbf{E}$.
5. Reattach the shaft to the pickup unit. Reattach the pu. shaft holder to the shaft using the screw $\mathbf{D}$.


Fig. 16


Fig. 13


Fig. 14


Fig. 15


Fig. 17

## - Removing the trigger arm

## (See Fig. 18 and 19)

- Prior to performing the following procedure, remove the top cover, the connector board and the clamper unit.

1. Turn the trigger arm in the direction of the arrow to release the joint $\mathbf{k}$ and pull out upward.

CAUTION: When reassembling, insert the part I and $\mathbf{m}$ of the trigger arm into the part $\mathbf{n}$ and 0 at the slot of the chassis rivet assembly respectively and join the joint $k$ at a time.


Fig. 19

## - Removing the top plate assembly

(See Fig.20)

- Prior to performing the following procedure, remove the top cover, the connector board, the chassis unit, and the clamper assembly.

1. Remove the screw $\mathbf{H}$.
2. Move the top plate assembly in the direction of the arrow to release the two joints $\mathbf{p}$.
3. Unsolder the wire marked $\mathbf{q}$ if necessary.


Fig. 20

## ■Removing the select arm (L) / select lock arm (See Fig. 21 and 22)

- Prior to performing the following procedure, remove the top plate assembly.

1. Bring up the select arm (L) to release from the link plate (joint $\mathbf{r}$ ) and turn in the direction of the arrow to release the joint $\mathbf{s}$.
2. Unsolder the wire of the select arm (L) marked $\mathbf{q}$ if necessary.
3. Turn the select lock arm in the direction of the arrow to release the two joints $t$.

The select lock arm spring comes off the select lock arm at the same time.

## -Reassembling the select arm (L) / select lock arm (See Fig. 23 to 25)

REFERENCE: Reverse the above removing procedure.

1. Reattach the select lock arm spring to the top plate and set the shorter end of the select lock arm spring to the hook $\mathbf{u}$ on the top plate.
2. Set the other longer end of the select lock arm spring to the boss $\mathbf{v}$ on the underside of the select lock arm, and join the select lock arm to the slots (joint $\mathbf{t}$ ). Turn the select lock arm as shown in the figure.
3. Reattach the select arm (L) while setting the part $\mathbf{r}$ to the first peak of the link plate gear, and join the joint s.

CAUTION: When reattaching the select arm (L), check if the points $\mathbf{w}$ and $\mathbf{x}$ are correctly fitted and if each part operates properly.
(imarer


Fig. 24


Fig. 21

Fig. 22
Select lock arm spring


Fig. 23
-


Fig. 25

## Removing the select arm (R) / link plate

 (See Fig. 21 and 22)- Prior to performing the following procedure, remove the top plate assembly.

1. Bring up the select arm (R) to release from the link plate (joint $\mathbf{y}$ ) and turn as shown in the figure to release the two joints $\mathbf{z}$ and joint $\mathbf{a}^{\prime}$.
2. Move the link plate in the direction of the arrow to release the joint b'. Remove the link plate spring at the same time.

REFERENCE:Before removing the link plate, remove the select arm (L).

## - Reattaching the Select arm (R) / link plate (See Fig. 25 and 26)

REFERENCE: Reverse the above removing procedure.

1. Reattach the link plate spring.
2. Reattach the link plate to the link plate spring while joining them at joint b'.
3. Reattach the part $y$ of the select arm (R) to the first peak of the link plate while joining the two joints $\mathbf{z}$ with the slots. Then turn the select arm (R) as shown in the figure. The top plate is joined to the joint $\mathbf{a}^{\prime}$.

CAUTION: When reattaching the select arm (R), check if the part $\mathbf{c}$ ' is correctly fitted and if each part operates properly.


Fig. 21


Fig. 22


Fig. 25


Fig. 26

Removing the loading roller assembly (See Fig. 27 to 29)

- Prior to performing the following procedure, remove the clamper assembly and the top plate assembly.

1. Push inward the loading roller assembly on the gear side and detach it upward from the slot of the joint d' of the lock arm rivet assembly.

Detach the loading roller assembly from the slot of the joint e' of the lock arm rivet assembly.

The roller guide comes off the gear section of the loading roller assembly.

Remove the roller guide and the washer from the shaft of the loading roller assembly.
2. Remove the screw I attaching the lock arm rivet assembly.
3. Push the shaft at the joint f' of the lock arm rivet assembly inward to release the lock arm rivet assembly from the slot of the slide plate. Extend the lock arm rivet assembly outward and release the joint $g^{\prime}$ from the boss of the chassis rivet assembly. The roller guide springs on both sides come off.

CAUTION: When reassembling, reattach the left and right roller guide springs to the lock arm rivet assembly before reattaching the lock arm rivet assembly to the chassis rivet assembly. Make sure to fit the part $\mathbf{h}$ ' of the roller guide spring (L) inside of the roller guide (Refer to Fig.30).


Fig. 30


Fig. 27


Joint $\mathrm{h}^{\prime}$


Fig.28-1
Loading roller assembly


Fig.28-2


Fig. 29

Removing the loading gear (5), (6) and (7) (See Fig. 31 and 32)

- Prior to performing the following procedure, remove the top cover, the chassis unit and the top plate assembly.

1. Remove the screw $\mathbf{J}$ attaching the loading gear bracket. The loading gear (6) and (7) come off the loading gear bracket.
2. Pull out the loading gear (5).


Fig. 31


Fig. 32

## ■Removing the gears (See Fig. 33 to 36)

- Prior to performing the following procedure, remove the top cover, the chassis unit, the top plate assembly and the pickup unit.

1. Pull out the feed gear.
2. Move the loading plate assembly in the direction of the arrow to release the slide plate from the two slots j' of the chassis rivet assembly.
3. Detach the loading plate assembly upward from the chassis rivet assembly while releasing the joint $\mathbf{k}$. Remove the slide hook and the loading plate spring from the loading plate assembly.
4. Pull out the loading gear (2) and remove the change lock lever.
5. Remove the E-washer and the washer attaching the changer gear (2).
6. The changer gear (2), the changer gear spring and the adjusting washer come off.
7. Remove the loading gear (1).
8. Move the hang plate rivet assembly in the direction of the arrow to release from the three shafts of the chassis rivet assembly upward.
9. Detach the loading gear plate rivet assembly from the shaft of the chassis rivet assembly upward while releasing the joint l'.
10. Pull out the loading gear (4).


Fig. 33


Fig. 34


Fig. 35

## ■Removing the turn table / spindle motor

 (See Fig. 37 and 38)- Prior to performing the following procedure, remove the top cover, the connector assembly and the chassis / clamper assembly.

1. Remove the two screws $\mathbf{K}$ attaching the spindle motor assembly through the slot of the turn table on top of the body.
2. Unsolder the wire on the connector board if necessary.


Fig. 37


Fig. 38

## Adjustment method

Test instruments required adjustment
1.Digital oscilloscope ( 100 MHz )
2.AM Standard signal generator
3.FM Standard signal generator
4.Stereo modulator
5. Electric voltmeter
6.Digital tester
7.Test disc(CTS-1000)
8.Extension cable for check

EXTGS004-22P

Standard volume position
Balance and Bass \& Treble volume : Indication "0" Loudness : OFF

Frequency Band
FM $87.5 \mathrm{kHz}-108.0 \mathrm{kHz}$

AM (MW) $522 \mathrm{kHz}-16200 \mathrm{kHz}$
(LW) 144kHZ-279kHz

Dummy load
Exclusive dummy load should be used for AM, and FM.
For FM dummy load, there is a loss of 6 dB between SSG output and antenna input. The loss of 6 dB need not be considered since direct reading of figures are applied in this working standard.

Standard measuring conditions
Power supply voltage DC $14.4 \mathrm{~V}(11 \mathrm{~V}$ to 16 V allowance)
Load impedance $4 \Omega(4 \Omega$ to 8 Sallowance)
Line-out Level/Impedance
: $2.0 \mathrm{~V} / 20 \mathrm{k} \Omega$ load(full scale)
Output impedance : $1 \mathrm{k} \Omega$


## Flow of functional operation unit TOC read



Feed section


## Focus section



- Spindle section



## -Tracking section



## Maintenance of laser pickup

(1) Cleaning the pickup lens

Before you replace the pickup,please try to clean the lens with a alcohol soaked cotton swab.
(2) Life of the laser diode

When the life of the laser diode has expired. the following symptoms will appear.
(1) The level of RF output (EFM output:amplitude of eye patterrn) will be low.


## Replacement of laser pickup

(3) Semi-fixed resistor on the APC PC board The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power. Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor. If the laser power is lower than the specified value, the laser diode is almost worn out, and the laser pickup should be replaced. If the semi-fixed resistor is adjusted while the pickup is functioning normally, the laser pickup may be damaged due to excessive current.

Turn of the power switch and, disconnect the power cord.


## Description of major ICs

BA3220FV-X (IC301,IC401) : Line out amp
1.Pin layout

2.Block diagram


## UPD784217AGC177 (IC701) : CPU

1. Pin layout

| 75 | $\sim$ | 51 |
| :---: | :---: | :---: |
| $\stackrel{\circ}{1}$ |  | $\bigcirc$ |
| , |  | 2 |
| 은 |  | $\stackrel{\circ}{\circ}$ |
| 1 | $\sim$ | 25 |

2. Pin function (1/2)

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1~5 | NC | - | Non connect |
| 6 | CD-MUTE | 0 | CD MUTE |
| 7 | CD-REST | 0 | CD REST |
| 8 | ANT REM | 0 | Antenna remote output |
| 9 | VDD | - | 5 V connection |
| 10 | X2 | - | Connect to X'tal for main clock |
| 11 | X1 | - | Connect to X'tal for main clock |
| 12 | VSS | - | Connect to GND |
| 13 | XT2 | - | Connect to X'tal for sub clock |
| 14 | XT1 | - | Connect to X'tal for sub clock |
| 15 | RESET | 1 | Reset detection terminal |
| 16 | P.REQ | 0 | Mechanism power supply ON/OFF demand output ("L" on demand) |
| 17 | BUS-INT | 1 | J-BUS signal interrupt input |
| 18 | PS2 | 1 | Power save 2 |
| 19 | NC | - | Non connect |
| 20 | RDS-SCK | 1 | Clock input for RDS |
| 21 | RDS-DA | 1 | RDS data input |
| 22 | REMOCON | 1 | Remocon signal input |
| 23 | AVDD | 1 | 5 V connect |
| 24 | AVREFO | 1 | 5 V connect |
| 25 | SD/ST | 1 | Station detector, Stereo signal input |
| 26 | MRC DATA | 1 | MRC data input |
| 27 | KEYO | 1 | Key input 0 |
| 28 | KEY1 | - | Key input 1 |
| 29 | TEMP | 1 | Temperature data input for contrast correction |
| 30 | LEVEL | - | Level meter input |
| 31 | SQ | 1 | S.quality level input |
| 32 | S.METER | 1 | S.meter level input |
| 33 | AVSS | - | Connect to GND |
| 34 | INLOCK | 1 | Lock detection output |
| 35 | NC | 0 | Non connect |
| 36 | AVREF | I/O | 5 V connect |
| 37 | BUS-SI | 1 | J-BUS data input |
| 38 | BUS-SO | 0 | J-BUS data output |
| 39 | BUS-SCK | 0 | J-BUS clock input/output |
| 40 | LCD-CE1 | 0 | Chip enable 1 out put for LCD driver |
| 41 | LCD-DA | 0 | Data output for LCD driver |
| 42 | LCD-CL | 0 | Clock output to LCD driver |
| 43 | LCD-CE2 | 0 | Chip enable 2 out put for LCD driver |
| 44 | BUZZER | 0 | Buzzer output |
| 45 | EPDAI | I | Communication data input 12C |

2. Pin function (2/2)

UPD784217AGC177

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 46 | EP-DAO | 0 | Communication data input of 12C |
| 47 | EPCLK | 0 | Communication data input of 12C |
| 48 | BUS-I/O | 0 | J-BUS I/O switching output |
| 49 | PM0 | 0 | Panel close side motor control signal output |
| 50 | PM1 | 0 | Panel open side motor control signal output |
| 51 | EQ-CLK | 0 | Equalizer clock |
| 52 | EQ-DA | 0 | Equalizer data |
| 53 | EQ-LA | 0 | Equalizer latch |
| 54 | STAGE | 1 | H:L: Initialization port |
| 55 | VCR CONT | 0 | VCR control signal output |
| 56~61 | PNL-SW1~6 | 1 | Panel position detection switch 1 to 6 signal input |
| 62 | AFCK | 0 | AF clock output |
| 63 | SEEK/STOP | O | SEEK:H STOP:L |
| 64 | S.MUTE | 0 | Signal mute output |
| 65 | FM/AM | 0 | FM / AM select output |
| 66 | PLL-CE | 0 | PLL IC control CE output |
| 67 | PLL-DO | 0 | PLL IC control data output |
| 68 | PLL-CLK | 0 | PLL IC control clock output |
| 69 | PLL-DI | I | PLL IC control data input |
| 70 | TEL MUTE | I | Telephone mute signal detection input |
| 71 | AMP KILL | I | Amp off signal input |
| 72 | VSS | - | Connect to GND |
| 73 | DIMMER-IN | I | Dimmer detection input |
| 74 | PS1 | I | Power save 1 |
| 75 | POWER | 0 | Power ON / OFF select output |
| 76 | CD-ON | - | Non connect |
| 77 | MUTE | 0 | Mute output |
| 78 | W-LPF1 | 0 | Sub woofer cut off frequency control output 1 |
| 79 | W-LPF2 | 0 | Sub woofer cut off frequency control output 2 |
| 80 | W-MUTE | 0 | Sub woofer mute output |
| 81 | VDD | O | 5 V connect |
| 82 | VOL-DA | 0 | E. volume IC control data output |
| 83 | VOL-CLK | O | E. volume IC control clock data output |
| 84 | CF SEL | O | FM band area filter select signal output |
| 85 | PMKICK | O | Panel motor kick signal output |
| 86 | SELECT | - | Non connect |
| 87 | DIM-CONT | 0 | Dimmer control signal output |
| 88 | VOL-1 | 1 | Rotary volume pulse |
| 89 | VOL-2 | I | Rotary volume pulse signal input |
| 90 | $\mathrm{J} / \mathrm{U}$ | I | Pull down |
| 91 | NC | - | Non connect |
| 92 | NC | - | Non connect |
| 93 | NC | - | Non connect |
| 94 | TEST | 1/O | Connect to GND |
| 95 | NC | - | Non connect |
| 96 | NC | - | Non connect |
| 97 | NC | - | Non connect |
| 98 | NC | - | Non connect |
| 99 | DISCSEL | 0 | $\mathrm{H}: 8 \mathrm{~cm}$ disc non correspondence $\mathrm{L}: 8 \mathrm{~cm}$ disc correspondence |
| 100 | NC | - | Non connect |

## UPD784225GK-623 (IC501) : CPU

1.Pin layout

| $61^{60}$ | ~ | ${ }^{41} 40$ |
| :---: | :---: | :---: |
| $\sim$ |  | $\sim$ |
| ${ }^{80} 1$ | $\sim$ | $20^{21}$ |

2.Pin functions (1/2)

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1 | TEMP IN | I | Temp. detection input terminal |
| 2,3 | - | - | No use |
| 4 | AVSS | - | Connect to GND |
| 5 | ADCONT | 0 | Output H level at power to on |
| 6 | - | - | - |
| 7 | AVREF1 | - | Connect to 3.3V |
| 8 | EPROMDI | 1 | EEPROM data input terminal |
| 9 | EPROMDO | 0 | EEPROM data output terminal |
| 10 | EPROMCK | 1/0 | EEPROM clock signal input/output terminal |
| 11 | LCD CE | 0 | Chip enable output for LCD driver |
| 12 | LCD DA | 0 | Data output for LCD driver |
| 13 | LCD CK | 0 | Clock outout for LCD driver |
| 14 | BUS I/O | 0 | JVC BUS input/output control terminal (negative) |
| 15 | BUS I/O | 0 | JVC BUS input/output control terminal |
| 16 | BUS SI | 1 | JVC BUS data input terminal |
| 17 | BUS SO | O | JVC BUS data output terminal |
| 18 | BUS SCK | I/O | JVC BUS clock input/output terminal |
| 19 | BUSOUT | 0 | JVC BUS BUSOUT output terminal |
| 20 | CD ON | 0 | Power supply (3.3V) control for CD |
| 21 | CD REQ | 0 | CD mechanism power supply to on request signal output terminal |
| 22 | CD MUTE | O | CD mute signal output terminal |
| 23 | - | - | - |
| 24 | DSP RESET | 0 | CD DSP reset signal output terminal |
| 25 | CCE | 0 | CD DSP chip enable output terminal |
| 26 | BUCK | 0 | CD DSP data clock output terminal |
| 27 | BUS3 | 1/0 | CD DSP data 3 input/output terminal |
| 28 | BUS2 | I/O | CD DSP data 2 input/output terminal |
| 29 | BUS1 | 1/0 | CD DSP data 1 input/output terminal |
| 30 | BUSO | I/O | CD DSP data 0 inout/output terminal |
| 31 | 2X PLAY | 0 | RF frequency responce select output of 2xspeed playback |
| 32 | RW SEL | 0 | CD-RW select output terminal (RW:L) |
| 33 | VSS1 | - | Connect to GND |
| 34 | LD | 0 | Loading signal output terminal |
| 35 | LD/FE | 0 | Loading/Feed select signal output terminal (H:LD,L:FE) |
| 36 | MP3 DI | 1 | CD MP3 data input terminal |
| 37 | MP3 DO | 0 | CD MP3 data output terminal |
| 38 | MP3 CK | 0 | Clock signal output terminal for CD MP3 data |
| 39 | MP3 RESET | 0 | CD MP3 reset signal output terminal |
| 40 | MP3 STB | 0 | CD MP3 standby signal output terminal (H:Standby) |
| 41~43 | - | - | - |
| 44 | DAC ML | 0 | DAC mode control latch output terminal |
| 45 | DAC MC | 0 | DAC mode control BCK output terminal |
| 46 | DAC MD | 0 | DAC mode control data output terminal |

2.Pin functions (2/2)

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :--- |
| 47 | DAC CS | O | DAC chip select terminal |
| $48 \sim 51$ | - | - | No use |
| 52 | DISC SEL | I | 8cm disc corespondance mode select terminal (respondance:L) |
| 53 | DAC SEL | I | DAC select mode input terminal |
| 54 | - | - | - |
| 55 | TEST MODE | I | LCD/AD key/Remocon invalid select mode input terminal L:invalid |
| 56 | MP3 SEL | I | MP3 select mode input terminal |
| 57 | 8 V DET | I | CD mechanism power supply detection terminal (L:8V on) |
| 58 | REST | I | CD mechanism rest switch input terminal |
| 59 | SW2 | I | CD mechanism SW2 input terminal |
| 60 | RESET | I | Riset signal input terminal |
| 61 | SW1 | I | CD mechanism SW1 input terminal |
| 62 | B.DET | I | Backup power supply detection input terminal (H:Stop mode) |
| 63 | P.DET | I | Main power off detection input terminal (H:HALT mode) |
| 64 | BUS INT | I | JVC BUS comunication start squeeze input terminal |
| 65 | MP3 REQ | I | CD MP3 request signal input terminal |
| 66 | - | - | - |
| 67 | VSS0 | - | Connect to GND |
| 68 | VDD1 | - | Connect to 3.3V |
| 69 | X2 | O | Ocsillator (6MHz) |
| 70 | X1 | I | Oscillator (6MHz) |
| 71 | VPP | - | Connec to GND |
| 72 | XT2 | O | Open |
| 73 | XT1 | I | Connect to GND |
| 74 | VDD0 | - | Connect to 3.3V |
| 75 | AVDD | - | Connect to ADCONT |
| 76 | IOP | I | Pickup IOP measurment input terminal |
| 77 | KEY0 | I | Key input 0 (8bit A/D input) terminal |
| 78 | KEY1 | I | Key input 1 (8bit A/D input) terminal |
| 79 | KEY2 | I | Key input 2 (8bit A/D input) terminal |
| 80 | KET3 | I | Key input 3 (8bit A/D input) terminal |
|  |  |  |  |

## LA6579H-X (IC681) : 4-Channel bridge driver

1. Pin layout \& Block diagram

3.Pin function

| Pin No. | Symbol |  |
| :---: | :--- | :--- |
| 1 | VIN1-A | CH1 input AMP_inverted input |
| 2 | VIN1+A | CH1 input AMP_non-inverted input |
| 3 | VCCP1 | CH1 and CH2 power stage power supply |
| 4 | VO1+ | Output pin(+)ffor channel 1 |
| 5 | VO1-- | CH1 output pin (-) for channel 1 |
| 6 | VO2+ | Output pin(+)for channel 2 |
| 7 | VO2- | Output pin(-)for channel 2 |
| 8 | VO3+ | Output pin(+)for channel 3 |
| 9 | VO3- | Output pin(--)for channel 3 |
| 10 | VO4+ | Output pin(+)for channel 4 |
| 11 | VO4- | Output pin(--)for channel 4 |
| 12 | VCCP2 | CH3 and CH4 power stage powr supply |
| 13 | VIN4 | Input pin for channel 4 |
| 14 | VIN4G | Input pin for channel 4(for gain adjustment) |
| 15 | VIN3 | Input pin for channel 3 |
| 16 | VIN3G | Input pin for channel 3(for gain adjustment) |
| 17 | VIN2 | Input pin for channel 2 |
| 18 | VIN2G | Input pin for channel 2(for gain adjustment) |
| 19 | REGIN | External PNP transistor, base connection |
| 20 | $3.3 V R E G$ | 3.3VREG output pin, external PNP transistor,collector connection |
| 21 | VCCS | Signal system GND |
| 22 | VREFIN | Reference voltage application pin |
| 23 | MUTE | Output ON/OFF pin |
| 24 | VIN1_SW | CH1 input OP AMP_changeover pin |
| 25 | S_GND | Signal system GND |
| 26 | VIN1+B | CH1 AMP_B non-inverted input pin |
| 27 | VIN1-B | CH1 AMP_B inverted input pin |
| 28 | VIN1 | CH1 input pin, input OP_AMP output pin |

## IC-PST9333U-X (IC702) : Regulator

1. Pin layout

2. Block diagram


## 3. Pin function

| Pin No. | Symbol | Function |
| :---: | :---: | :--- |
| 1 | NC | Non connect |
| 2 | GND | GND terminal |
| 3 | VOUT | Reset signal output terminal |
| 4 | Vcc | Vcc terminal/Voltage detect terminal |

## TA2157FN-X (IC601) : RF amp

1.Terminal layout
$\left\{\begin{array}{ccc|}\hline 24 & \sim & 13 \\ 1 & \sim & 12 \\ \hline\end{array}\right.$

## 2.Block diagram



| PIN | SEL <br> (APC SW) | TEB <br> (TE BAL) | RFGC <br> (AGC Gian) | TEB <br> (TE BAL) |
| :---: | :---: | :---: | :---: | :---: |
| VCC | APC ON | $-50 \%$ | +12 dB | Normal mode <br> $(0 \mathrm{~dB})$ |
| HiZ | APC ON | $0 \%$ | +6 dB | Normal mode <br> $(0 \mathrm{~dB})$ |
| GND | APC OFF <br> $($ LDO $H)$ | $+50 \%$ | 0 dB | CD-RW mode <br> $(+12 \mathrm{~dB})$ |

3.Pin function

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1 | VCC | - | 3.3V power supply pin |
| 2 | FNI | 1 | Main-beam amp input pin |
| 3 | FPI | 1 | Main-beam amp input pin |
| 4 | TPI | 1 | Sub-beam amp input pin |
| 5 | TNI | 1 | Sub-beam amp input pin |
| 6 | MDI | 1 | Monitor photo diode amp input pin |
| 7 | LDO | 0 | Laser diode amp output pin |
| 8 | SEL | I | APC circuit ON/OFF control signal, laser diode (LDO) control signal input or bottom/peak detection frequency change pin. |
|  |  |  | SEL APC <br> circuit LCD |
|  |  |  | GND $\quad$ OFF $\quad$ Connected VCC through 1k resistor |
|  |  |  | Hiz ON Control signal output |
|  |  |  | VCC |
| 9 | TEBC | I | Tracking error balance adjustment signal input pin <br> Adjusts TE signal balance by ellminating carrier component from PWM signal (3-state output,PWM carrier $=88.2 \mathrm{kHz}$ ) output from TC94A14F/FA TEBC pin using RC-LPF and inputting DC. <br> TEBC input voltage:GND~VCC |
| 10 | TEN | 1 | Tracking error signal genaration amp negative-phase input pin |
| 11 | TEO | O | Tracking error signal generation amp output pin. Combining TEO signal RFRP signal with TC94A14F/FA configures tracking search system. |
| 12 | RFDC | 0 | RF signal peak detection output pin |
| 13 | GVSW | I | AGC/FE/TE amp gain change pin |
|  |  |  | GVSW Mode |
|  |  |  | GND CD-RW |
|  |  |  | Hiz Normal |
|  |  |  | VCC |
| 14 | VRO | 0 | Reference voltage (VRO) output pin *VRO=1/2VCC When VCC=3.3V |
| 15 | FEO | 0 | Focus error signal generation amp output pin |
| 16 | FEN | 1 | Focus error signal generation amp negative-phase input pin |
| 17 | RFRP | O | Signal amp output pin for track count Combining RFRP signal and TEO signal with TC94A14F/FA configures tracking search system. |
| 18 | RFRPIN | 1 | Signal generation amp input pin for track count |
| 19 | RFGO | 0 | RF signal amplitude adjustment amp output pin |
| 20 | RFGC | I | RF amplitude adjustment control signal input pin <br> Adjusts RF signal amplitude by eliminating carrier component from PWM signal (3-state output,PWM carrier=88.2kHz)output fromTC94A14F/14FA RFGC pin using RC-LPF and inputting DC. <br> * RFGC input voltage:GND~VCC |
| 21 | AGCIN | 1 | RF signal amplitude adjustment amp input pin |
| 22 | RFO | 0 | RF signal generation amp output pin |
| 23 | RFN | 1 | RF signal generation amp input pin |
| 24 | GND | - | GND pin |

## TC94A14FA (IC621) : DSP \& DAC

1.Terminal layout \& block daiagram

2.Pin function

| Pin <br> No | Symbol | I/O | Descroption |
| :---: | :---: | :---: | :--- |
| 1 | BCK | O | Bit clock output pin.32fs,48fs,or 64fs selectable by command. |
| 2 | LRCK | O | LR channel lock output pin."L" for L channel and "H" for R channel. Output polarity <br> can be inverted by command. |
| 3 | AOUT | O | Audio data output pin. MSB-first or LSB-first selectable by command. |
| 4 | DOUT | O | Digital data output pin.Outputs up to double-speed playback. |
| 5 | IPF | O | Correction flag output pin. When set to "H", AOUT output cannot be corrected by C2 <br> correction processing. |
| 6 | VDD3 | - | Digital 3.3V power supply voltage pin. |
| 7 | VSS3 | - | Digital GND pin. |
| 8 | SBOK | O | Subcode Q data CRCC result output pin. "H" level when result is OK. |
| 9 | CLCK | O | Subcode P-W data read I/O pin. I/O polarity selectable by command. |
| 10 | DATA | O | Subcode P-W data output pin. |
| 11 | SFSY | O | Playback frame sync signal output pin. |
| 12 | SBSY | O | Subcode block sync signal output pin. "H" level at S1 when subcode sync is detected. |
| 13 | HSO | I/O | General-purpose input / output pins. <br> Input port at reset. |
| 14 | UHSO |  |  |
| 15 | PVDD3 | - | PLL-only 3.3V power supply voltage pin. |


| $\begin{aligned} & \text { Pin } \\ & \text { No } \end{aligned}$ | Symbol | I/O | Description |
| :---: | :---: | :---: | :---: |
| 16 | PDO | 0 | EFM and PLCK phase difference signal output pin. |
| 17 | TMAX | O | TMAX detection result output pin. |
|  |  |  | TMAX Detection Result ${ }^{\text {T }}$ TMAX Output |
|  |  |  | Longer than fixed period "PVDD3" $^{\text {a }}$ |
|  |  |  | Within fixed period |
|  |  |  | Shorter than fixed period |
| 18 | LPFN | 1 | Inverted input pin for PLL LPF amp. |
| 19 | LPFO | 0 | Output pin for PLL LPF amp. |
| 20 | PVREF | - | PLL-only VREF pin. |
| 21 | VCOF | 0 | VCO filter pin. |
| 22 | AVSS3 | - | Analog GND pin. |
| 23 | SLCO | 0 | DAC output pin for data slice level generation. |
| 24 | RFI | 1 | RF signal input pin. Zin selectable by command. |
| 25 | AVDD3 | - | Analog 3.3 V power supply voltage pin. |
| 26 | RFCT | I | RFRP signal center level input pin. |
| 27 | RFZI | 1 | RFRP signal zero-cross input pin. |
| 28 | RFRP | I | RF ripple signal input pin. |
| 29 | FEI | 1 | Focus error signal input pin. |
| 30 | SBAD | I | Sub-beam adder signal input pin. |
| 31 | TEI | 1 | Tracking error input pin. Inputs when tracking servo is on. |
| 32 | TEZI | 1 | Tracking error signal zero-cross input pin. |
| 33 | FOO | 0 | Focus equalizer output pin. |
| 34 | TRO | 0 | Tracking equalizer output pin. |
| 35 | VREF | - | Analog reference power supply voltage pin. |
| 36 | RFGC | 0 | RF amplitude adjustment control signal output pin. |
| 37 | TEBC | 0 | Tracking balance control signal output pin. |
| 38 | SEL | O | APC circuit ON/OFF signal output pin. At laser on, high impedance with UHS="L", H output with UHS="H". |
| 39 | AVDD3 | - | Analog 3.3V power supply voltage pin. |
| 40 | FMO | 0 | Feed equalizer output pin. |
| 41 | DMO | 0 | Disc equalizer output pin. |
| 42 | VSS3 | - | Digital GND pin. |
| 43 | VDD3 | - | Digital 3.3V power supply voltage pin. |
| 44 | TESIN | 1 | Test input pin. Normally, fixed to "L". |
| 45 | XVSS3 | - | System clock oscillator GND pin. |
| 46 | XI | 1 | System clock oscillator input pin. |
| 47 | XO | 0 | System clock oscillator output pin. |
| 48 | XVDD3 | - | System clock oscillator 3.3V power supply voltage pin. |
| 49 | DVSS3R | - | DA converter GND pin. |
| 50 | RO | 0 | R-channel data forward output pin. |
| 51 | DVDD3 | - | DA converter 3.3 V power supply pin. |
| 52 | DVR | - | Reference voltage pin. |
| 53 | LO | 0 | L-channel data forward output pin. |
| 54 | DVSS3L | - | DA converter GND pin. |
| 55 | ZDET | 0 | 1 bit DA converter zero detection flag output pin. |
| 56 | VSS5 | - | Microcontroller interface GND pin. |
| 57 | BUSO |  |  |
| 58 | BUS1 | I/O | Microcontroller interface data I/O pins. |
| 59 | BUS2 |  |  |
| 60 | BUS3 |  |  |
| 61 | BUCK | 1 | Microcontroller interface clock input pin. |
| 62 | /CCE | 1 | Microcontroller interface chip enable signal input pin.At "L", BUS0 to BUS3 are active. |
| 63 | /RST | 1 | Reset signal input pin. At reset, "L". |
| 64 | VDD5 | - | Microcontroller interface 5V power supply pin. |

■ TC94A02F-005 (IC652) : DSP

3.Pin function(1/2)

TC94A02F-005

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1 | /RESET | 1 | Hard reset input terminal(H:Normal operation L: Reset) |
| 2 | MiMD | 1 | Micon I/F mode select input terminal |
| 3 | AD0 | O | External SRAM address output 0 terminal |
| 4 | AD1 | 0 | External SRAM address output 1 terminal |
| 5 | MiDio | I/O | Micon I/F data input/output terminal |
| 6 | /MiCK | 1 | Micon I/F clock input terminal |
| 7 | AD2 | 0 | External SRAM address output 2 terminal |
| 8 | VDDT | - | Digital power supply (3.3V) |
| 9 | SDo | 0 | Data output terminal |
| 10 | AD3 | 0 | External SRAM address output 3 terminal |
| 11 | AD4 | 0 | External SRAM address output 4 terminal |
| 12 | SDi0 | 1 | Data input terminal 0 |
| 13 | BCKiA | 1 | Bit clock input terminal A |
| 14 | LRCKiA | 1 | LR clock input terminal A |
| 15 | AD5 | 0 | External SRAM address output 5 terminal |
| 16 | CE | 0 | External SRAM chip enable terminal |
| 17 | OE | 0 | External SRAM output enable terminal |
| 18 | VDD | - | Digital power supply (2.5V) |
| 19 | STANBY | 1 | Standby mode control terminal |
| 20 | VSS | - | Digital GND |
| 21 | VSSL | - | DAC Lch GND |
| 22 | VRAL | - | DAC Lch reference voltage terminal |
| 23 | LO | 0 | DAC Lch output terminal |
| 24 | VDAL | - | DAC Rch power supply terminal(2.5V) |
| 25 | VDAR | - | DAC Lch power supply terminal(2.5V) |
| 26 | RO | 0 | DAC Rch output terminal |
| 27 | VRAR | - | DAC Rch reference voltage terminal |
| 28 | VSSR | - | DAC Rch GND |
| 29 | TESTP | 1 | Test terminal |
| 30 | CKS | 1 | VCO select terminal |
| 31 | AD12 | 0 | External SRAM address output 12 terminal |
| 32 | AD11 | 0 | External SRAM address output 11 terminal |
| 33 | AD10 | 0 | External SRAM address output 10 terminal |
| 34 | AD9 | 0 | External SRAM address output 9 terminal |
| 35 | VDDT | - | Digital power supply terminal (3.3V) |
| 36 | AD8 | 0 | External SRAM address output 8 terminal |
| 37 | AD7 | 0 | External SRAM address output 7 terminal |
| 38 | AD6 | 0 | External SRAM address output 6 terminal |
| 39 | REQ | 0 | Squeeze request terminal to host |
| 40 | VSS | - | Digital GND |
| 41 | AD13 | 0 | External SRAM address output 13 terminal |
| 42 | AD14 | 0 | External SRAM address output 14 terminal |
| 43 | WR | 0 | External SRAM write signal |
| 44 | AD16 | 0 | External SRAM address output 16 terminal |
| 45 | AD15 | 0 | External SRAM address output 15 terminal |
| 46 | io 0 | I/O | External SRAM data input/output 0 terminal |
| 47 | $i 01$ | I/O | External SRAM data input/output 1 terminal |
| 48 | VSS | - | Digital GND |
| 49 | io2 | I/O | External SRAM data input/output 2 terminal |
| 50 | io3 | I/O | External SRAM data input/output 3 terminal |

3.Pin function(2/2)

| Pin No. | Symbol | I/O |  |
| :---: | :---: | :---: | :--- |
| 51 | io4 | I/O | External SRAM data input/output 4 terminal |
| 52 | VDD | - | Digital power supply (2.5V) terminal |
| 53 | io5 | I/O | External SRAM data input/output 5 terminal |
| 54 | io6 | I/O | External SRAM data input/output 6 terminal |
| 55 | io7 | I/O | External SRAM data input/output 7 terminal |
| 56 | VSSP | - | VCO GND |
| 57 | Pdo | O | PLL phase error detection signal output terminal |
| 58 | Vcoi | I | VCO control voltage input terminal |
| 59 | VDDP | - | VCO power supply |
| 60 | Cko | O | 16.934 MHz clock output terminal |
| 61 | VDDX | - | Power supply (2.5V) terminal for oscillator |
| 62 | Xi | I | Connection terminal for oscillator(input) |
| 63 | Xo | O | Connection terminal for oscillator(output) |
| 64 | VSSX | - | GND for oscillator |

## $\square$ HD74HC126FP-X (IC771) : Buffer

1.Pin layout

3.Block diagram

Note) CL includes probe and jig capacitance

## BA6956AN (IC495) : Reversible motor driver

1.Block diagram

2. Pin function

| Pin No. | Symbol | Function |
| :---: | :---: | :--- |
| 1 | VREF | Output high voltage level control terminal |
| 2 | OUT2 | Output terminal for motor |
| 3 | RNF | GND of driver division |
| 4 | OUT1 | Output terminal for motor |
| 5 | VM | Power supply for driver division |
| 6 | Vcc | Power supply for signal division |
| 7 | FIN | Input terminal for control logic |
| 8 | GND | GND |
| 9 | RIN | Input terminal for control logic |

3. Truth table

| FIN | RIN | OUT1 | OUT2 | MODE |
| :---: | :---: | :---: | :---: | :--- |
| H | L | H | L | Forward rotation mode |
| L | H | L | H | Reverse rotation mode |
| H | H | L | L | Break Mode |
| L | L | OPEN | OPEN | Stand-by mode |

## ■BU4066BCFV-X (IC322,IC351) : Quad analog switch

1. Pin layout \& Block diagram


BR24C01AFV-W-X (IC502) : EEPROM

2.Block diagram

3.Pin function

| Pin name | I/O | Function |
| :---: | :---: | :--- |
| Vcc | - | Power supply |
| GND | - | Ground (Ov) |
| A0,A1,A2 | IN | Slave address set |
| SCL | IN | Serial clock input |
| SDA | IN / OUT | Slave and word address, <br> serial data input, serial data output *1 |
| WP | IN | Write protect input |

*1 An open drain output requires a pull-up resister.

## HA13164A (IC961) : Regulator

1.Terminal layout

2.Block diagram


UNIT R: R:
note1) TAB (header of IC)
connected to GND
3.Pin function

| Pin No. | Symbol | Function |
| :---: | :--- | :--- |
| 1 | EXTOUT | Output voltage is VCC-1 V when M or H level applied to CTRL pin. |
| 2 | ANTOUT | Output voltage is VCC-1 V when M or H level to CTRL pin and H level <br> to ANT-CTRL. |
| 3 | ACCIN | Connected to ACC. |
| 4 | VDDOUT | Regular 5.7V. |
| 5 | SW5VOUT | Output voltage is 5V when M or H level applied to CTRL pin. |
| 6 | COMPOUT | Output for ACC detector. |
| 7 | ANT CTRL | L:ANT output OFF , H:ANT output ON |
| 8 | VCC | Connected to VCC. |
| 9 | BATT DET | Low battery detect. |
| 10 | AUDIO OUT | Output voltage is 9V when M or H level applied to CTRL pin. |
| 11 | CTRL | L:BIAS OFF, M:BIAS ON, H:CD ON |
| 12 | CD OUT | Output voltage is 8V when H level applied to CTRL pin. |
| 13 | ILM AJ | Adjustment pin for ILM output voltage. |
| 14 | ILM OUT | Output voltage is 10V when M or H level applied to CTRL pin. |
| 15 | GND | Connected to GND. |

■ HD74HCT126T-X (IC503) : Buffer
1.Terminal layout

| $\stackrel{\text { c }}{ }$ | O | \% | な | O | ¢ |  | < |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | ¢ | $\cdots$ | $\cdots$ | 안 |  |  |  |

3.Pin function

| INPUT |  | OUTPUT |
| :---: | :---: | :---: |
| C | $A$ | $Y$ |
| $L$ | $X$ | $Z$ |
| $H$ | $L$ | $L$ |
| $H$ | $H$ | $H$ |

H: High level
L: Low level
X: Irrelevant
Z: Off (Hhigh-impedance)state of a 3-stage
2.Block diagram


LC75878W (IC801,IC802) : LCD driver

| 1. Pin layout | $100 \sim 76$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 |  |  |  | 75 |
|  | $\sim$ |  |  |  | $\sim$ |
|  | 25 |  |  |  | 51 |
|  |  | 26 | $\sim$ |  |  |


3. Pin function

| No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :--- |
| $1 \sim 73$ | SEG1~SEG73 | O | Segment driver output pin. |
| 74 | SEG74 | O | Segment driver output pin. |
| 75 | SEG75 | O | Segment driver output pin. |
| $76 \sim 83$ | COM8~COM1 | O | Common driver output pin. |
| $84 \sim 87$ | P1~P4 | O | General-purpose output pin. |
| 88 | VDD | - | Logic block power supply pin. |
| 89 | VLCD | - | LCD driver power supply pin. |
| 90 | VLCD0 | O | LCD driver bias 4/4 voltage (H-level) power pin. |
| 91 | VLCD1 | I | LCD driver bias 3/4 voltage (intermediate level) power pin. |
| 92 | VLCD2 | I | LCD driver bias 2/4 voltage (intermediate level) power pin. |
| 93 | VLCD3 | I | LCD driver bias 1/4 voltage (intermediate level) power pin. |
| 94 | VLCD4 | I | LCD driver bias 0/4 voltage (L-level) power pin. |
| 95 | VSS | - | Power supply pin to connect to ground. |
| 96 | OSC | I/O | Oscillator pin. |
| 97 | LCD RESET | I | Display off, general-purpose output port "L" fixed input pin. |
| 98 | CE | I | Chip enable |
| 99 | CL | I | Synchronization clock |
| 100 | DI | I | Transfer data |

M62449FP-X (IC912) : Equalizer


NJM4565V-X (IC171,IC323,IC572,IC951) : Dual ope amp
1.Terminal layout \& Pin function


1 AOUTPUT
2 A-INPUT
3 A+INPUT
$4 \mathrm{~V}^{-}$
5 B+INPUT
6 B-INPUT
7 B OUTPUT
$8 \mathrm{~V}^{+}$

## NJU7241F25-X (IC651) : Regulator

1.Pin layout

2.Block diagram


## W24L010AJ-AS-X (IC653) : SRAM


2.Block diagram

3.Pin functions

| Symbol | Function |
| :---: | :--- |
| A0-A16 | Address inputs |
| l/O1-l/O8 | Data inpts/outputs |
| CS1,CS2 | Chip select input |
| WE | Write enable input |
| OE | Output enable input |
| VDD | Power supply |
| VSS | Ground |
| NC | No connection |

## ■ PCM1716E-X (IC571) : D/A converter

1. Pin layout

2. Block diagram

3. Pin function

| Pin <br> No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :--- |
| 1 | LRCK | I | LRCK clock input |
| 2 | DATA | I | Serial audio data input |
| 3 | BCK | I | Bit clock input for serial audio data |
| 4 | CLKO | O | Buffered output of system clock |
| 5 | XTI | I | Oscillator input / External clock input |
| 6 | XTO | O | Oscillator output |
| 7 | DGND | - | Digital ground |
| 8 | VDD | - | Digital power +5 V |
| 9 | VDD2R | - | Analog power +5 V |
| 10 | AGND2R | - | Analog ground |
| 11 | EXTR | O | Rch common pin of analog output amp |
| 12 | NC | - | Non connection |
| 13 | VOUTR | O | Rch analog voltage output of audio signal |
| 14 | AGND1 | - | Analog ground |
| 15 | Vcc1 | - | Analog power +5 V |
| 16 | VOUTL | O | Lch analog voltage output of audio signal |
| 17 | NC | - | Non connection |
| 18 | EXTL | O | Lch common pin of analog output amp |
| 19 | AGND2L | - | Analog ground |
| 20 | Vcc2L | - | Analog power +5 V |
| 21 | ZERO | O | Zero data flag |
| 22 | RST | I | Reset |
| 23 | CS/IWO | I | Chip select / Input format selection |
| 24 | MODE | I | Mode control select |
| 25 | MUTE | I | Mute control |
| 26 | MD/DM0 | I | Mode control, Data / De-emphasis selection 1 |
| 27 | MC/DM1 | I | Mode control, BCK / De-emphasis selection 2 |
| 28 | ML/IIS | I | Mode control, WDCK / Input format selection |

RPM6938-SV4 (IC861) : Remote sensor
1.Block diagram


■ TDA7404D-X (IC911) : Carradio signal processor
1.Termnal layout

2..Block diagram


## SAA6579T-X (IC51) : RDS

1.Pin layout

3.Pin function
2.Block diagram


| Pin No. | Symbol | Function |
| :---: | :--- | :--- |
| 1 | QUAL | Quality indication output |
| 2 | RDDA | RDS data output |
| 3 | Vref | Reference voltage output (0.5VDDA) |
| 4 | MUX | Multiolex signal input |
| 5 | VDDA | +5V supply voltage for analog part |
| 6 | VSSA | Ground for analog part (0V) |
| 7 | CIN | Subcarrier input to comparator |
| 8 | SCOUT | Subcarrier output of reconstruction filter |
| 9 | MODE | Oscllator mode / test control input |
| 10 | TEST | Test enable input |
| 11 | VSSD | Ground for digital part (0V) |
| 12 | VDDD | +5V supply voltage for digital part |
| 13 | OSCI | Oscillator input |
| 14 | OSCO | Oscillator output |
| 15 | T57 | 57 kHz clock signal output |
| 16 | RDCL | RDS clock output |

## ■ NJU7241F33-X (IC504) : Voltage regulator



PIN FUNCTION

1. GND
2. Vin
3. Vout
4. +NC
5. STB

## TB2901H (IC941) : Power amp

1.Terminal layout

2.Block diagram


