AsahiKASEI
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AK7600

2/6-Channel Audio CODEC with Digital EQ

GENERAL DESCRIPTION

AK7600 is a CODEC (2ch ADC, 6ch DAC) with a delay line memory and digital filters such as EQ. This device operates in master mode and the internal sampling rate is 44.1kHz. It supports 5.0V single input and the integrated regulator generates the internal voltage. The 2-channeled ADC achieves dynamic rage of 97dB single end inputs, and 6-channeled DAC achieves 102dB single end outputs. The delay line memory covers 36ms in total. Time alignment of 6m or less is possible since the delay line memory can store for 18ms data for both left and right channels. A car audio system can be built easily 5-bands EQ and time alignment functions.

FEATURES

1. **2ch 24bit ADC**
   - **64times Over Sampling**
   - **Linear Phase Digital Anti-Alias Filter**
   - **Single-ended input**
   - **S/(N+D): 90dB**
   - **DR, S/N: 97dB**
   - **Digital HPF for AC coupling**
2. **6ch 24bit DAC**
   - **128times Over Sampling**
   - **8times 24bit Digital filter**
   - **Single-ended output**
   - **S/(N+D): 90dB**
   - **DR, S/N: 102dB**
3. **Digital Processing**
   - **5Band EQ×2ch (Second-order IIR-filter setting is also available)**
   - **Delay line memory control**
     Maximum delay time:
     Max 36ms / Lch 18ms, Rch 18ms (1input and 3outputs for each channel)
     Adjustable output time (1/fs step)
   - **X'Over filter: 2step 2nd-order IIR Filter for Each channel of Delay line memory**
   - **Spectrum analyzer: 7Band**
     68Hz, 160Hz, 400Hz, 1kHz, 2.5kHz, 6.3kHz,16kHz
   - **Soft Mute**
   - **Zero Detect Function**
4. **Master Clock**
   - **Master Mode: 256fs**
5. **μP Interface: I^2C Bus (Ver 1.0, 400kHz mode)**
6. **Power Supply**
   - **Analog: AVDD = 4.5 ~ 5.5V**
   - **Digital: DVDD = 4.5 ~ 5.5V**
7. **Power Consumption: 52mA (fs=44.1kHz)**
8. **Ta = - 40 ~ 85°C**
9. **Package: 30VSOP(0.65mm pitch)**

■ Block Diagram

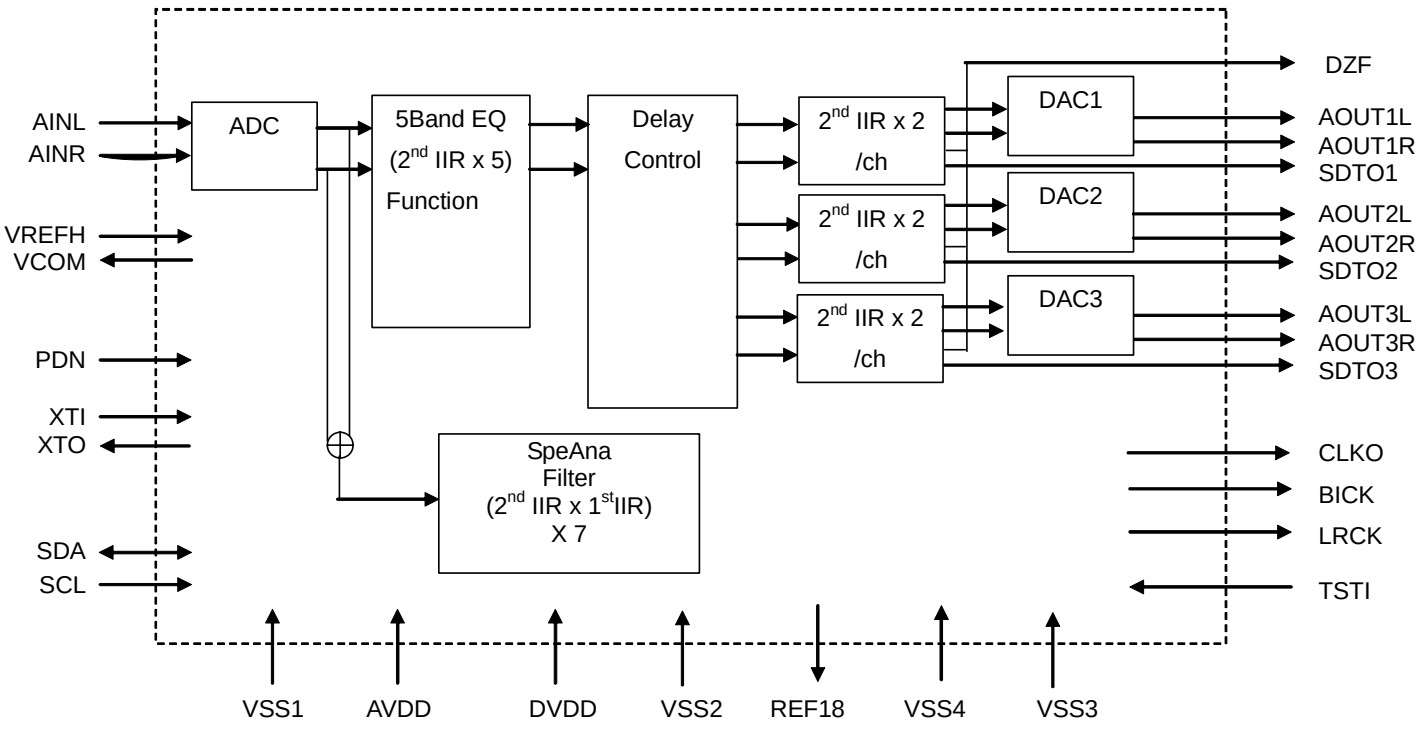


Figure 1. Block Diagram

■ Ordering Guide

AK7600VF	-40 ~ +85°C	30pin VSOP(0.65mm pitch)
AKD7600	Evaluation board for AK7600	

■ Pin Layout

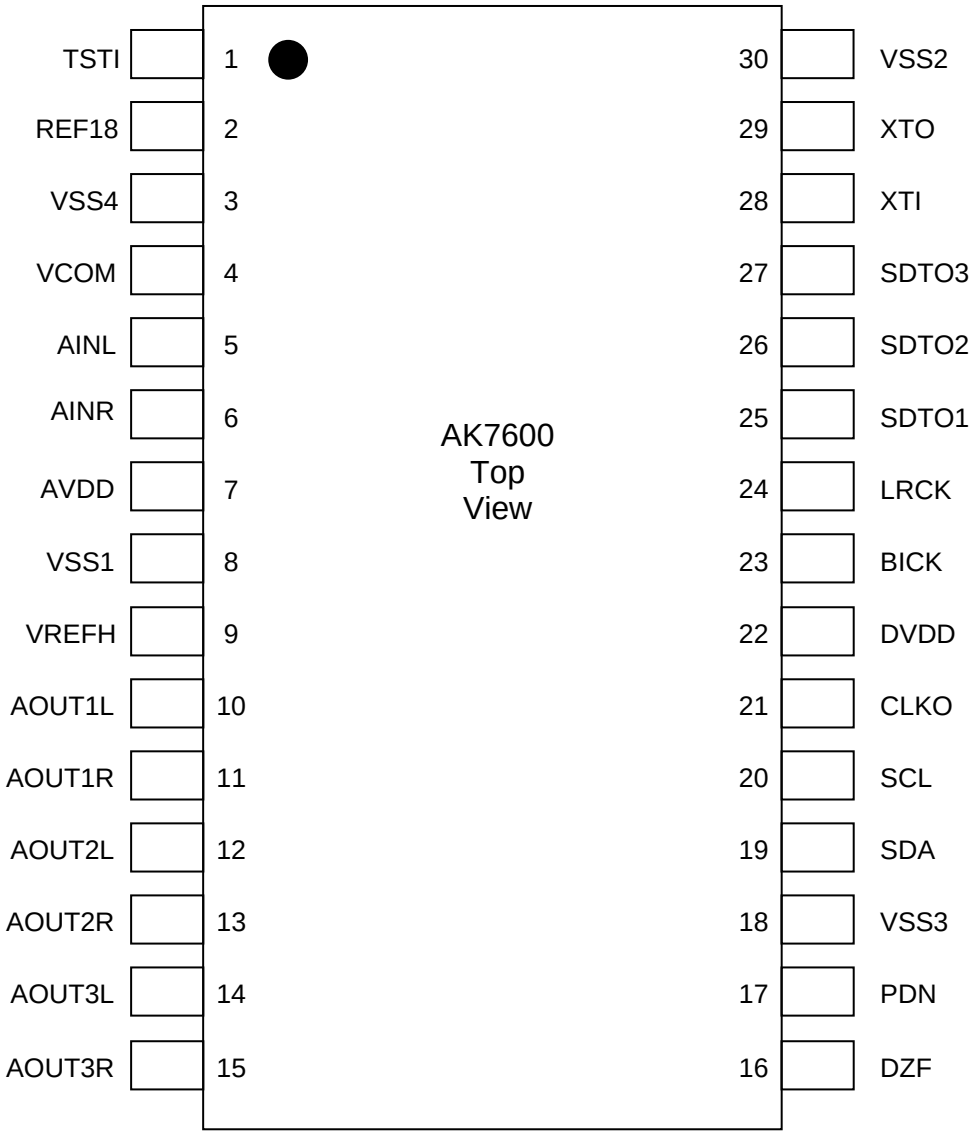


Figure 2. Pin Layout

PIN FUNCTION

No.	Pin Name	I/O	Function
1	TSTI	I	Test Pin This pin should be connected to VSS1.
2	REF18	O	Internal regulator 1.8V Output pin
3	VSS4	-	Ground Pin, 0V
4	VCOM	O	VCOM pin
5	AINL	I	ADC Input pin Lch.
6	AINR	I	ADC Input pin Rch
7	AVDD	-	Analog Power Supply Pin 4.5~5.5V
8	VSS1	-	Ground Pin, 0V
9	VREFH	-	Positive Voltage Reference Input Pin, AVDD
10	AOUT1L	O	DAC1 Lch Output pin.
11	AOUT1R	O	DAC1 Rch Output pin
12	AOUT2L	O	DAC2 Lch Output pin
13	AOUT2R	O	DAC2 Rch Output pin
14	AOUT3L	O	DAC3 Lch Output pin
15	AOUT3R	O	DAC3 Rch Output pin
16	DZF	O	Zero detect pin
17	PDN	I	Power-Down & Reset Pin When "L", the AK7600 is powered-down and the control registers are reset to default state.
18	VSS3	-	Ground Pin 0V
19	SDA	I/O	Control Data Input Pin : SDA (I^2C Bus) (Note 2)
20	SCL	I	Control Data Clock Pin : SCL (I^2C Bus)
21	CLKO	O	Master Clock Output Pin
22	DVDD	-	Digital Power Supply 1 Pin, 4.5~5.5V
23	BICK	O	Output Audio Serial Data Clock Pin
24	LRCK	O	Output Channel Clock Pin
25	SDTO1	O	Audio Serial Data Output 1 Pin
26	SDTO2	O	Audio Serial Data Output 2 Pin
27	SDTO3	O	Audio Serial Data Output 3 Pin
28	XTI	I	X'tal Input Pin
29	XTO	O	X'tal Output Pin
30	VSS2	-	Ground Pin, 0V

Note 1. All digital input pins are never to be left float.
Note 2. Input mode when powered-down.

■Handling of Unused Pin

The unused I/O pins should be processed appropriately as below

Classification	Pin Name	Setting
Analog	AOUT1L, AOUT1R, AOUT2L, AOUT2R, AOUT3L, AOUT3R, XTO	These pins should be open.
Digital	TSTI	This pin should be connected to VSS1.
	BICK, LRCK, CLKO, SDTO1, SDTO2, SDTO3	These pins should be open.

ABSOLUTE MAXMUM RATING

(VSS1=VSS2=VSS3=VSS4=0V; Note 3)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 3. All indicated voltages are with respect to ground VSS1, VSS2, VSS3 and VSS4 must be connected to the analog ground plane.

Note 4. Analog input pins are AINL and AINR.

Note 5. Digital input pins are TSTI, SDA, SCL and XTI.

WARNING: Operating at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these critical conditions.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4 =0V; Note 3)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	4.5	5.0	5.5	V
(Note 6)	Digital	DVDD	4.5	5.0	5.5	V

Note 6. AVDD and DVDD must be the same voltage. The power up sequence between AVDD and DVDD is not critical but the PDN pin must be “L” until all power supplies are ON, then put the PDN pin to “H”. All power supplies of the AK7600 are must be ON. Do not turn any power supply off (means the same voltage as ground or floating) independently. When using the AK7600 with I²C bus, the power supply of the AK7600 must not be turned off unless the power supplies of the surrounding device are turned off.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=5.0V, DVDD =5.0V; VSS1=VSS2=VSS3=VSS4=0V; VREFH=AVDD, fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at 44.1kHz, ; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics (single inputs)						
Resolution					24	Bits
S/(N+D)	fs=44.1kHz BW=20kHz	-1dBFS	83	90		dB
		-60dBFS		35		
DR (-60dBFS with A-weighted)			90	97		dB
S/N (A-weighted)			90	97		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Input Voltage	AIN=0.65xVREFH		3.09	3.25	3.41	Vpp
Input Resistance			22	45		kΩ
Power Supply Rejection (Note 7)				50		dB
DAC Analog Output Characteristics (single outputs)						
Resolution					24	Bits
S/(N+D)	fs=44.1kHz BW=20kHz	-1dBFS		90		dB
		-60dBFS		39		
DR (-60dBFS with A-weighted)				102		dB
S/N (A-weighted)				102		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.65xVREFH		3.09	3.25	3.41	Vpp
Load Resistance (AC load)			5			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 7)				50		dB
ADC to DAC Characteristics (single outputs)						
Resolution					24	Bits
S/(N+D)	fs=44.1kHz BW=20kHz	-1dBFS	80	87		dB
		-60dBFS		34		
DR (-60dBFS with A-weighted)			87	96		dB
S/N (A-weighted)			87	96		dB

Note 7. PSR is applied to AVDD and DVDD with 1kHz, 50mVpp. This is the value of convoluted sinusoidal voltage of 1kHz and 50mVpp when the VREFH pin is held +5V.

Parameter		min	typ	max	Units
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD	fs=44.1kHz		46	69	mA
DVDD	fs=44.1kHz		6	9	mA
Power-down mode (PDN pin = "L")					
AVDD+DVDD	(Note 8)		300	450	μA

Note 8. The AK7600 is not operating. This value is when all the digital input pins including clocks are held to VSS2.

FILTER CHARACTERISTICS

(Ta= -40 ~ +85°C; AVDD=4.5~ 5.5V, DVDD=4.5~ 5.5V)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 9)	±0.1dB	PB	0	-	17.3	kHz
	−0.2dB		-	18.3	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband (Note 9)		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.04	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 10)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	−3dB	FR	-	0.86	-	Hz
	−0.1dB		-	5.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 9)	±0.06dB	PB	0	-	20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 9)		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 10)		GD	-	20	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 11)	20~20kHz	FR	-	±0.1	-	dB

Note 9. The passband and stopband frequencies scale with fs (system sampling rate). For example, when fs= 44.1kHz, DAC is PB=0.45412*fs (@±0.06dB).

Note 10. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC. This time is from the set of 24bit data to the input registers to the output of analog signal for DAC.

Note 11. The reference frequency of these responses is 1kHz.

DC CHARACTERISTICS

(Ta=-40°C~+85°C; AVDD= DVDD=4.5~5.5V)

Parameter	Symbol	Min	typ	max	Units
High-Level Input Voltage (XTI, TSTI pins)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage (XTI, TSTI pins)	VIL	-	-	30%DVDD	V
High-Level Input Voltage (PDN, SDA, SCL pins)	VIH	2.0			V
Low-Level Input Voltage (PDN, SDA, SCL, pins)	VIL	-	-	0.8	V
High-Level Output Voltage (SDTO1, SDTO2 ,SDTO3, LRCK, BICK, SDA CLKO, DZF pins: Iout=-100μA)	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (SDTO1, SDTO2, SDTO3, LRCK, BICK, CLKO, DZF pins: Iout= 100μA)	VOL	-	-	0.5	V
(SDA pins: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=-40~+85°C; AVDD=4.5~5.5V; DVDD=4.5~5.5V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	Min	typ	max	Units
Master Clock Timing					
Crystal Resonator					
Frequency	fXTAL	10		13	MHz
MCKO Output					
Frequency	fMCK	10		13	MHz
Duty cycle	dMCK	40	50	60	%
External Clock					
256fsn:	fCLK	10		13	MHz
Pulse Width Low	tCLKL	36			ns
Pulse Width High	tCLKH	36			ns
MCKO Output					
Frequency	fMCK	10		13	MHz
Duty cycle	dMCK	40	50	60	%
Audio Interface Timing (Master mode)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–20	-	20	ns
BICK "↓" to SDTO	tBSD	–20	-	20	ns

Note 12. "L" when using I^2C format.
Note 13. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 14)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 15)	tPD	150			ns

Note 14. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 15. The AK7600 can be reset by bringing the PDN pin = "L".
Note 16. I2C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

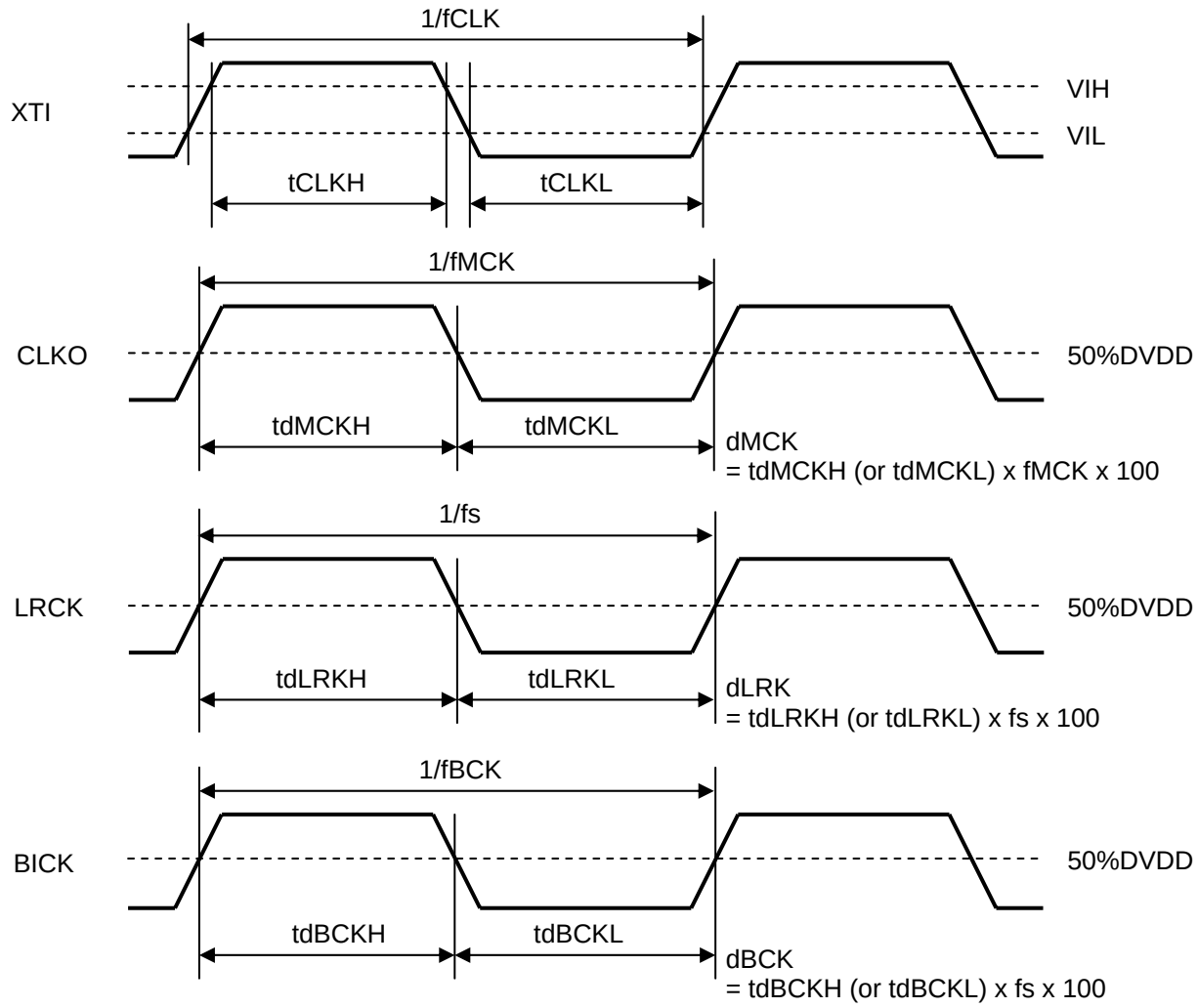


Figure 3. Clock Timing

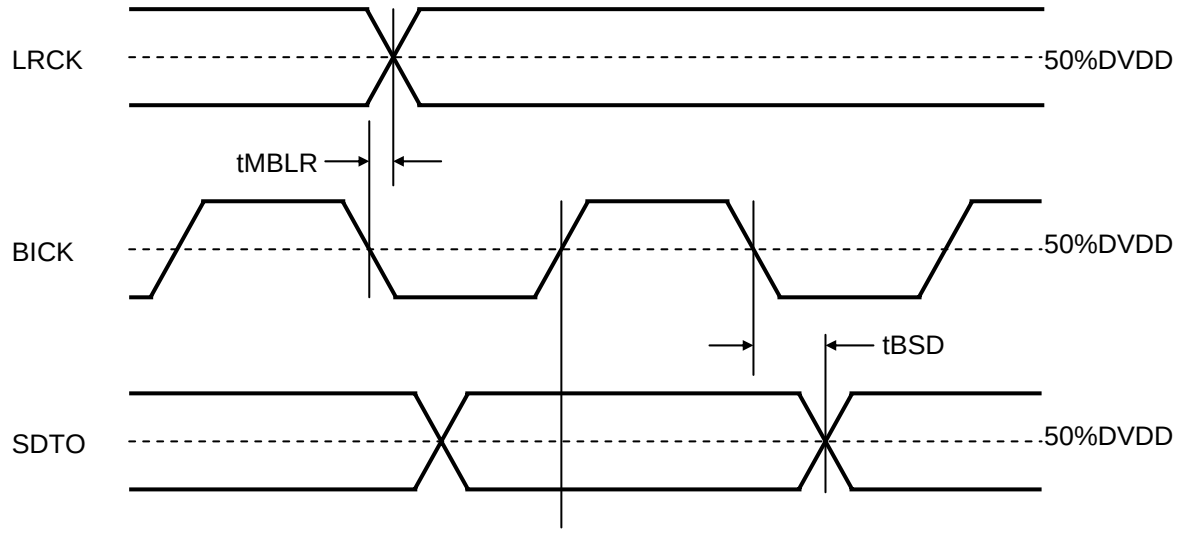


Figure 4. Audio Interface Timing (Master mode)

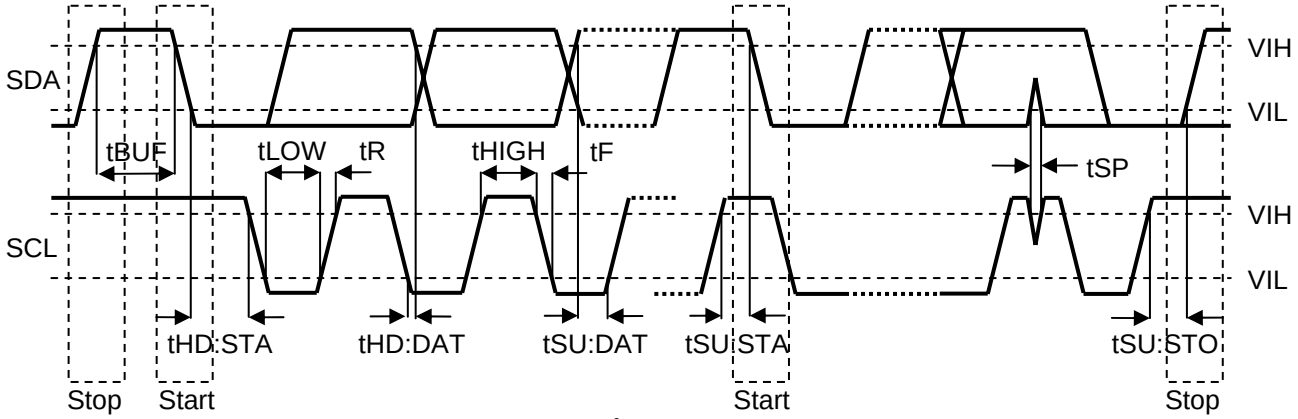


Figure 5. I^2C Bus Mode Timing

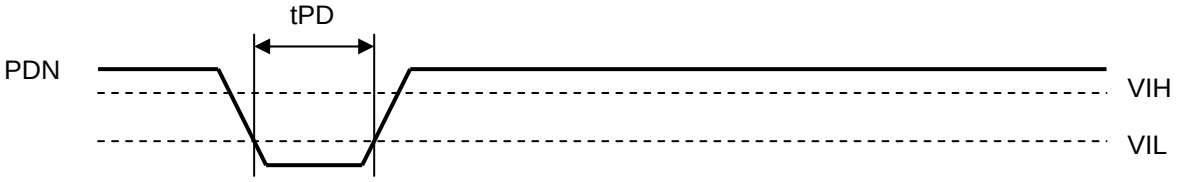


Figure 6. Power Down & Reset Timing

OPERATION OVERVIEW

■System Clock

The external clock input or X'tal input is available for MCLK clock source. (Figure 7, Figure 8) The required clock for master mode is 256fs MCLK only.

In the normal operation, if the clock is stopped, click noise may occur when the clock supply is restarted. It can be prevent by external mute.

LRCK	MCLK (MHz)	BICK (MHz)
fs	256fs	64fs
44.1kHz	11.2896	2.8224

Table 1. System Clock Example

■ Clock Source

The clock for the XTI pin can be generated by two methods:

1) External Clock

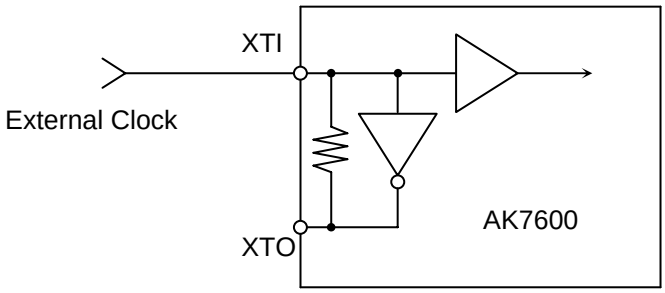


Figure 7. External Clock Mode

Note. Do not input the clock over DVDD.

2) X'tal

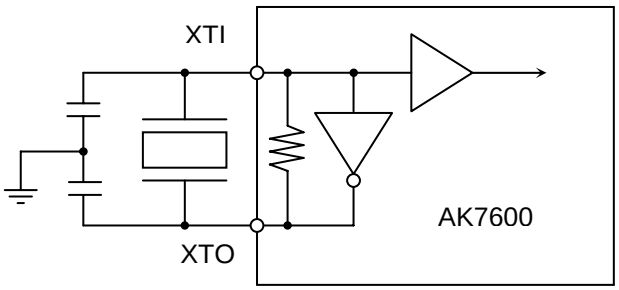


Figure 8. X'tal Mode

Note: The capacitor is dependent on X'tal value. (Typ.15pF)
When using X'tal, DVDD=4.5~5.5V.

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=44.1kHz). The frequency response scales with fs.

■ Master Clock Output Pin

CLKO is the output pin for master clock.

■ Audio Interface Format

The DIF pin can select between two serial data modes as shown in Table 2. In all modes the serial data is MSB-first, two's complement format and it is latched on the rising edge of BICK.

DIF Mode	SDTO1-3	LRCK		BICK		
			I/O		I/O	
0	24bit, Left justified	H/L	O	64fs	O	
1	24bit, I^{2}S	L/H	O	64fs	O	(default)

Table 2. Audio Data Format (Stereo mode)

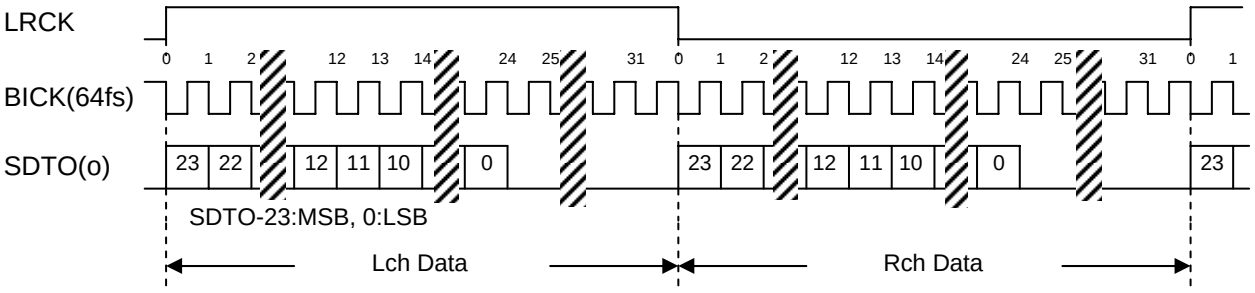


Figure 9. Mode 0 Timing (Left justified mode)

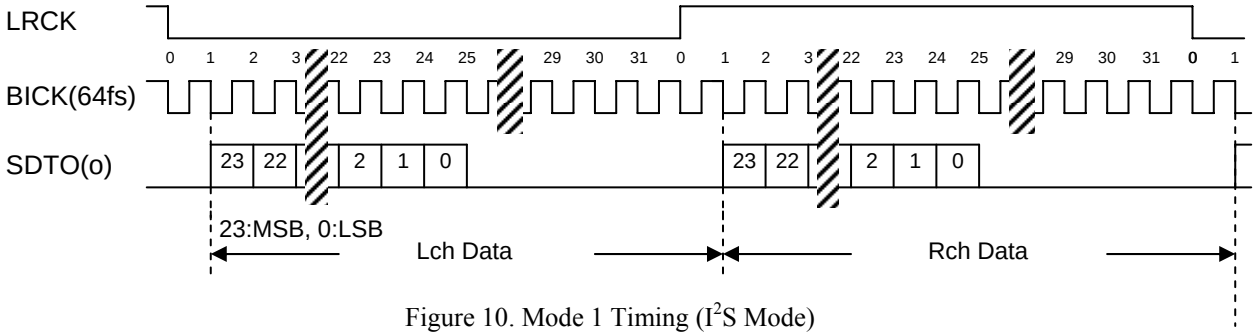


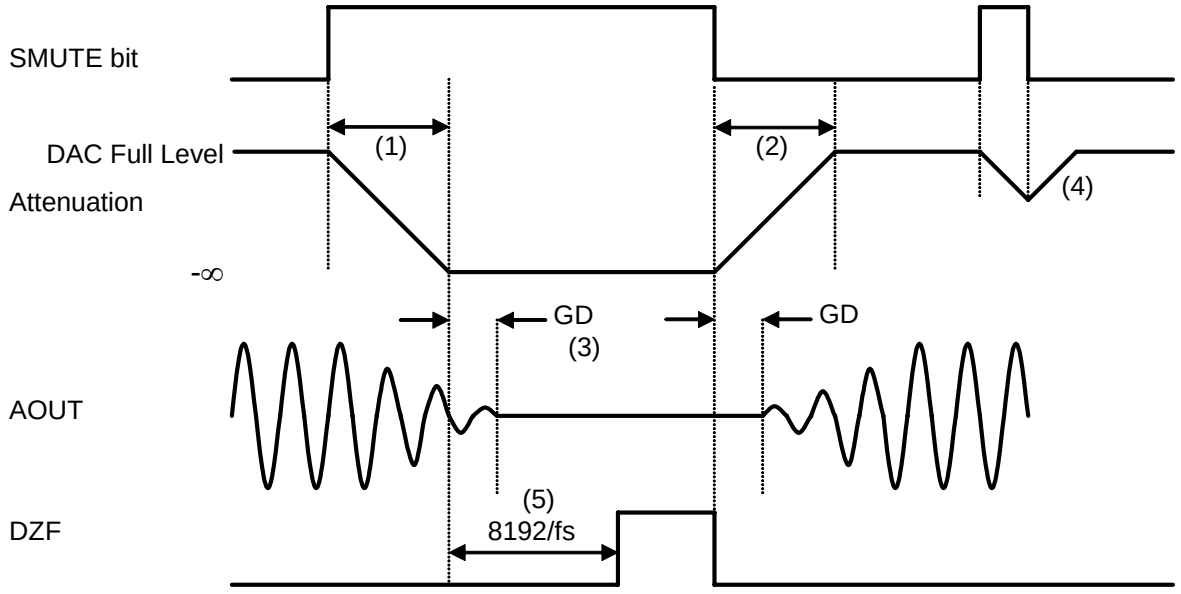
Figure 10. Mode 1 Timing (I^{2}S Mode)

■ Zero Detect Function

The AK7600 has independent zeros detect function for each DAC, which is always enabled. DZDD1-3 bits of CONT1 can select detection channel group and this function covers 6-channel outputs. Counting on "AND" for zero detected flags of selected channels, when the input data is continuously zeros for 8192 LRCK cycles, the DZF pin goes to "H" at DZLH bit (CONT1) is "0", the DZF pin goes to "L" at DZLH bit (CONT1) is "1". The DZF pin immediately returns to "L" (DZLH bit "0") or "H" (DZLH bit "1") if the input data is not zero after the zero detection.

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated to -∞ in 1024 LRCK cycles. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to 0dB in 1024 LRCK cycles. If the soft mute is cancelled within the 1024 LRCK cycles after starting this operation, the attenuation is discontinued and it is returned to 0dB by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.



Note:
(1) The transition time to attenuate input data to -∞ is 1024 LRCK cycles (1024/fs).
(2) The transition time to return to the full scale of the DAC input is 1024 LRCK cycles (1024/fs).
(3) Analog output corresponding to digital input has group delay (GD).
(4) If the soft mute is cancelled before attenuating -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
(5) When the input data for both channels are continuously zero for 8192 LRCK cycles, the DZF pin goes to "H". if the DZLH bit is "0" (the DZF pin goes to "L" if the DZLH bit is "1"). The DZF pin immediately returns to "L" if the input data are not zero after going to DZF "H" (DZLH bit ="0").

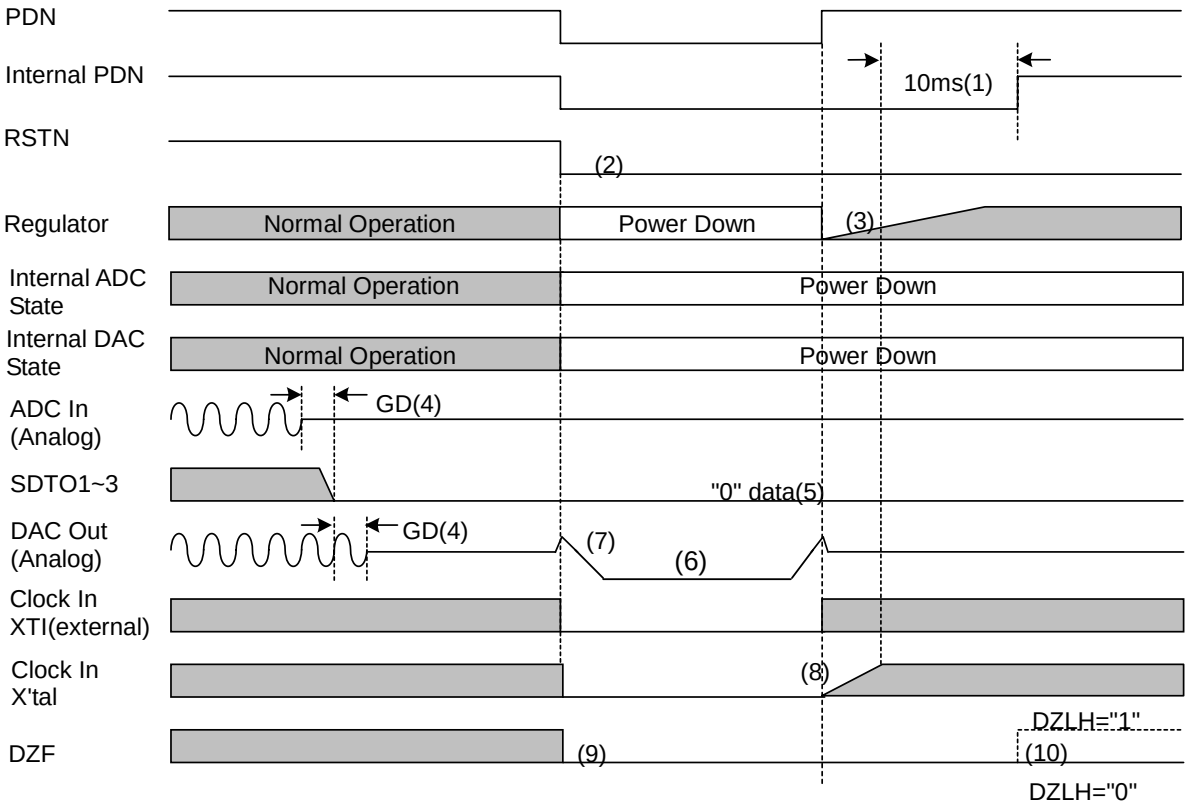
Figure 11 Soft Mute and Zero Detect Function

■ System Reset

The AK7600 should be reset once by bringing the PDN pin = "L" upon power-up. The regulator will be powered-up by inputting the master clock to the XTI pin directly or connect with a X'tal. The internal master clock starts by setting RSTN bit to "1" after an interval of 10ms.

■ Power Down

The ADC and DAC parts of the AK7600 are placed in the power-down mode by bringing the PDN pin "L" and the digital filter is also reset at the same time. The internal registers are initiated to their default value by the PDN pin = "L". This reset should always be made after power-up. In the power-down mode, SDTO1-3, BICK, LRCK and DZF pins go to "L" and the analog output is VSS. When exiting the power-down mode, the AK7600 will be in reset state since the RSTN bit = "0". Figure 12 shows the power on/off sequence example.



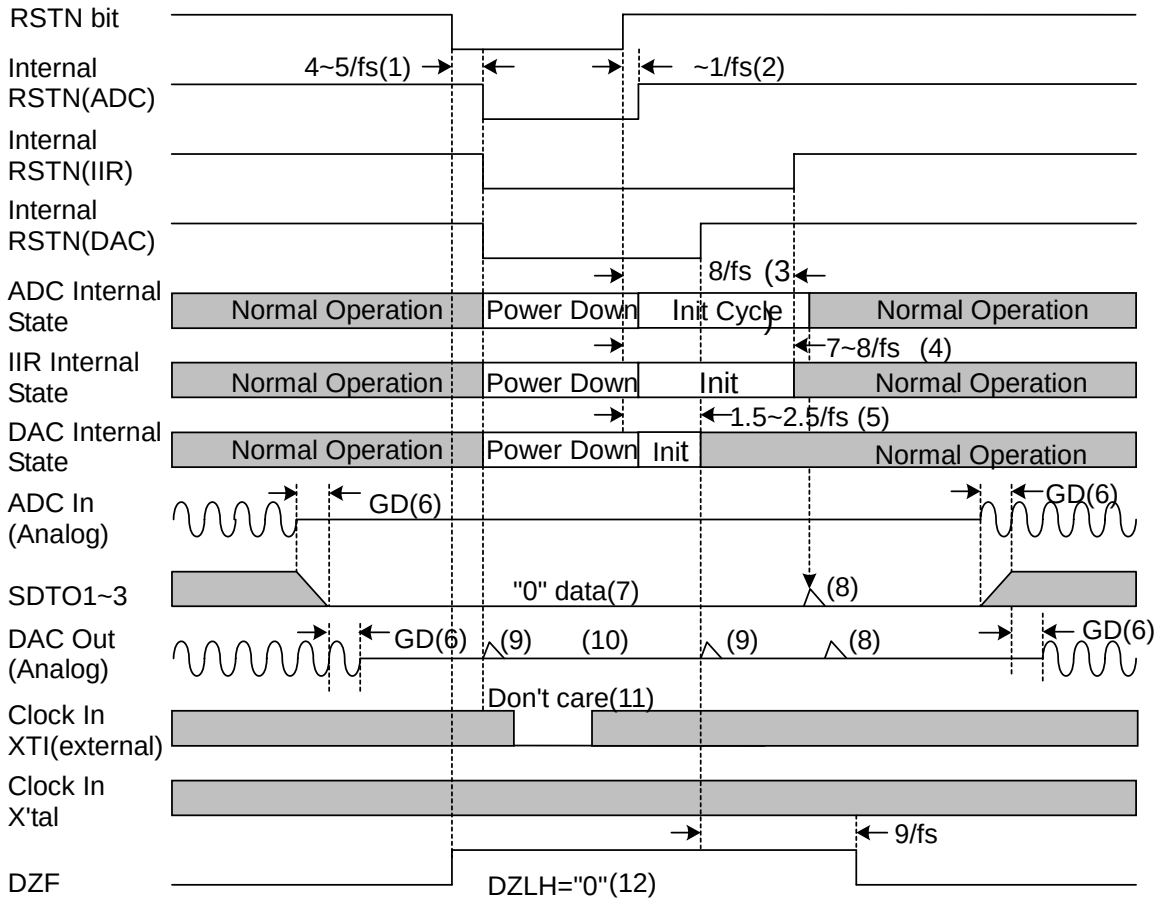
Note:

(1) After the PDN pin = "H", the internal PDN is "L" until X'tal and regulator are powered-up. (Register writing is not valid for 10ms of this period)
(2) During the RSTN bit is "0", all circuits will be powered down except the regulator and X'tal even when the internal PDN is "H".
(3) Regulator will be powered-up after the PDN pin goes to "H".
(4) The DAC and SDTO1-3 outputs corresponding to the ADC input has group delay (GD).
(5) The SDTP1-3 outputs are "0" when the AK7600 is powered-down.
(6) The DAC output is VSS voltage when the AK7600 is powered-down.
(7) Click noise occurs at the falling edge of PDN.
(8) In case of connecting a X'tal, the clock output is "L" when the PDN pin ="L". The X'tal will be powered up after the PDN pin ="H".
(9) In power down mode(PDN pin = "L"), the DZF pin = "L".
(10) The DZF pin output will reflects the DZLH bit setting when internal PDN is "H".

Figure 12. Power Up/Down Sequence Example

■ Reset Function

When the RSTN bit = "0", ADC and DAC parts of the AK7600 is powered down, but the internal register values are not initialized. The analog outputs settle to VCOM and the DZF pins for both channels go to "H" or "L" depending on the DZLH bit setting. SDTO1-3 pins go to "L" and analog output is VCOM voltage. Click noise occurs at this timing, mute the analog output externally if the click noise (8) influences system application. Figure 13 shows the example of reset by RSTN bit.



Note:

(1) Internal RSTN will be "L", 4~5/fs after RSTN bit went to "0".
(2) ADC internal RSTN will be "H", within 1/fs after RSTN bit = "1".
(3) The reset cycle is 8/fs after ADC internal RSTN goes to "H".
(4) Internal RSTN for IIR will be "H" after 7~8/fs from RSTN bit ="1".
(5) Internal RSTN for DAC will be "H" after 1.5~2.5/fs from RSTN bit = "1".
(6) The DAC and SDTO1-3 outputs corresponding to the ADC input has group delay (GD).
(7) SDTO1-3 output is "0" data when the AK7600 is in powered down mode.
(8) Click noise occurs when the initialization of ADC part is finished. Mute digital output if click noise adversely affects system performance.
(9) Click noise occurs at the edge of internal RSTN.
(10) Analog output is VCOM voltage(AVDD/2) when RSTN bit = "0".
(11) In case of inputting CLK from the XTI pin, the clock should be input before the RSTN bit is changed to "1" after the RSTN bit is set to "0".
(12) The DZF pin reflects the setting of DZLH bit. This pin changes to "L" or "H" 9/fs after the RSTN bit is set to "0".

Figure 13. Reset Sequence Example

■I²C BUS INTERFACE (Microcontroller Interface)

Access to the AK7600 registers and RAM is processed by I²C bus. The format of the I²C is complement with fast mode (max: 400kHz). The AK7600 does not support Hs mode. (max: 3.4MHz).

■ Data Transfer

In order to access any IC devices on the I²C BUS, input a start condition first, followed by a single Slave address which includes the Device Address. IC devices on the BUS compare this Slave address with their own addresses and the IC device which has an identical address with the Slave-address generates an acknowledgement. An IC device with the identical address then executes either a read or a write operation. After the command execution, input a Stop condition.

1-1. Data Change

Change the data on the SDA line while SCL line is "L". SDA line condition must be stable and fixed while the clock is "H". Change the Data line condition between "H" and "L" only when the clock signal on the SCL line is "L". Change the SDA line condition while SCL line is "H" only when the start condition or stop condition is input.

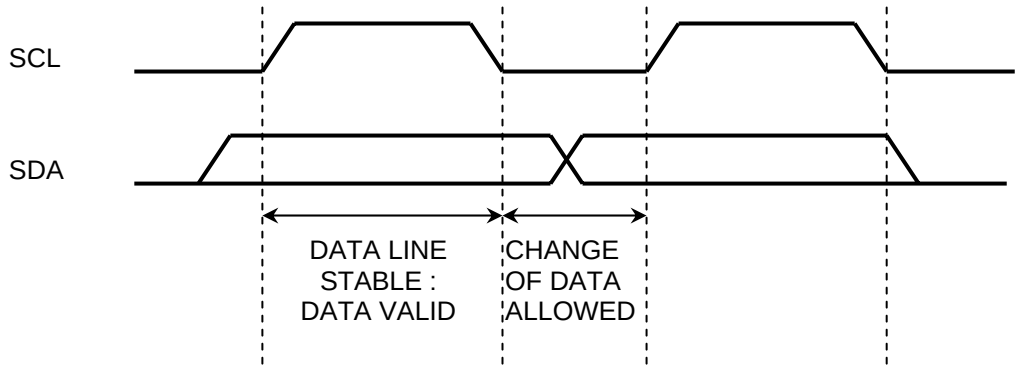


Figure 14. Data Transition

1-2. Start condition and Stop condition

Start condition is generated by the transition of "H" to "L" on the SDA line while the SCL line is "H". All instructions are initiated by Start condition. Stop condition is generated by the transition of "L" to "H" on SDA line while SCL line is "H". All instructions end by Stop condition.

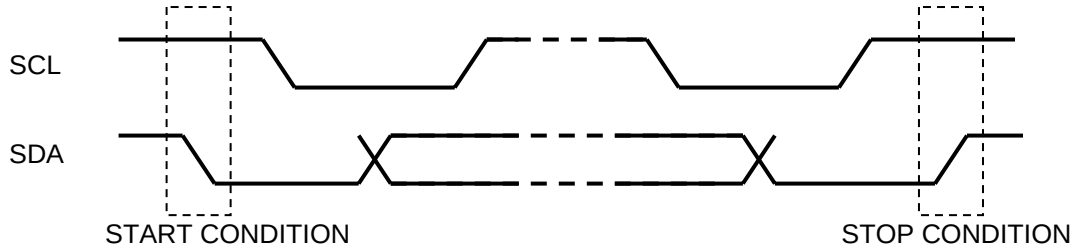


Figure 15. Start Condition and Stop Condition

1-3. Repeated Start Condition

When Start condition is received again instead of Stop condition, the bus changes to Repeated Start condition. Repeated Start condition is functionally the same as Start condition.

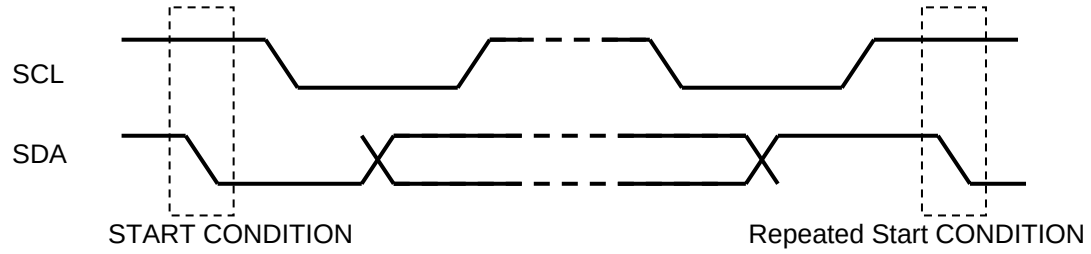


Figure 16. Repeated Start Condition

1-4. Acknowledge

An external device that is sending data to the AK7600 releases the SDA line ("H") after receiving one-byte of data. An external device that receives data from the AK7600 then sets the SDA line to "L" at the next clock. This operation is called "acknowledgement" and it enables verification that the data transfer has been properly executed. The AK7600 generates an acknowledgement upon receipt of Start condition and Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK7600 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the Master side generates an acknowledgement without sending Stop condition, the AK7600 outputs data at the next address location. When no acknowledgement is generated, the AK7600 ends data output (not acknowledged).

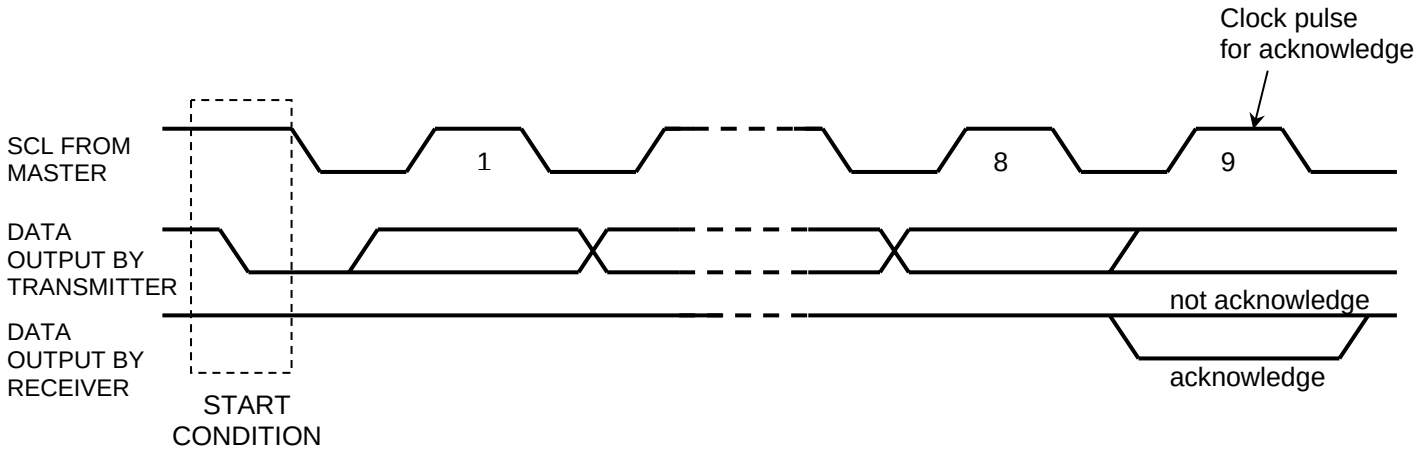


Figure 17. Acknowledge

1-5. The First byte

The First Byte which includes the Slave-address is input after the Start condition is set, and a target IC device that will be accessed on the bus is selected by the Slave-address. The Slave-address is configured with the upper 7-bits. Data of the upper 7-bits is "0011000". The address bits that select the desired IC are fixed. When the Slave-address is inputted, an external device that has the identical device address generates an acknowledgement and instructions are then executed. The 8th bit of the First Byte (lowest bit) is allocated as the R/W Bit. When the R/W Bit is "1", the read instruction is executed, and when it is "0", the write instruction is executed.

Note 17. In this document, there is a case that describes a "Write Slave-address assignment" when both address bits match and a Slave-address at R/W Bit = "0" is received. There is a case that describes "Read Slave-address assignment" when both address bits matches and a Slave-address at R/W Bit = "1" is received.

0	0	1	1	0	0	0	R/W

Slave Address is fixed 30H(write) or 31H(read).

Figure 18. The First Byte Structure

1-6. The Second and Succeeding Bytes

The data format of the second and succeeding bytes of the AK7600 Transfer / Receive Serial data (command code, address and data in microcontroller interface format) on the I2C BUS are all configured with a multiple of 8-bits. When transferring or receiving those data on the I2C BUS, they are divided into an 8-bit data stream segment and they are transferred / received with the MSB side data first with an acknowledgement in-between.

When transferring / receiving A1B2C3 (hex) 24-bit serial data in microprocessor interface format:

(1)I^2C Foormat

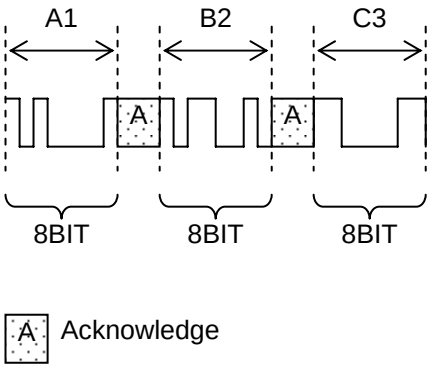


Figure 19. Division of the Data

Note 18. In this document, there is a case that describes a write instruction command code which is received at the second byte as "Write Command". There is a case that describes a read instruction command code which is received at the second byte as "Read Command"

■ Command Code

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
8/16/32 flag		Area to be accessed					

(1) 8/16/32 flag

When BIT[7:6] bits are "00", the following data will be 8bit. The data will be 16bit 10byte of 1word x 5 transfer when "01", and 32bit 20byte of 1word x 5 transfer when "10".

(2) Accompanying data to the access area

BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Command and Content
0	0	0	0	0	1	01H Control Register Cont0 Setting
0	0	0	0	1	0	02H Control Register Cont1 Setting
0	0	0	0	1	1	03H Control Register Cont2 Setting
0	0	0	0	0	0	40H Function2, Lch Coefficient Setting Preparation
0	0	0	0	0	1	41H Function2, Rch Coefficient Setting Preparation
0	0	0	0	1	0	42H Function2 Filter1 Coefficient Setting Preparation
0	0	0	0	1	1	43H Function2 Filter2 Coefficient Setting Preparation
0	0	0	1	0	0	44H Pre EQ ATT Coefficient Setting Preparation
0	0	0	1	0	1	45H EQ3 Filter Coefficient Setting Preparation
0	0	0	1	1	0	46H EQ4 Filter Coefficient Setting Preparation
0	0	0	1	1	1	47H X'Over ATT Coefficient Setting Preparation
0	0	1	0	0	0	48H X'Over Gain Coefficient Setting Preparation
0	0	1	0	0	1	49H Delay data Lch Setting Preparation
0	0	1	0	1	0	4AH Delay data Rch Setting Preparation
0	0	0	0	0	1	81H EQ0 Filter Coefficient Setting Preparation
0	0	0	0	1	0	82H EQ1 Filter Coefficient Setting Preparation
0	0	0	0	1	1	83H EQ2 Filter Coefficient Setting Preparation
0	0	0	1	0	0	84H X'Over HPF1-1 Coefficient Setting Preparation
0	0	0	1	0	1	85H X'Over HPF1-2 Coefficient Setting Preparation
0	0	0	1	1	0	86H X'Over HPF2-1 Coefficient Setting Preparation
0	0	0	1	1	1	87H X'Over HPF2-2 Coefficient Setting Preparation
0	0	1	0	0	0	88H X'Over LPF-1 Coefficient Setting Preparation
0	0	1	0	0	1	89H X'Over LPF-2 Coefficient Setting Preparation
0	0	0	0	0	1	C1H Read SpeAna 1Band (60Hz)
0	0	0	0	1	0	C2H Read SpeAna 2Band (160Hz)
0	0	0	0	1	1	C3H Read SpeAna 3Band (400Hz)
0	0	0	1	0	0	C4H Read SpeAna 3Band (1kHz)
0	0	0	1	0	1	C5H Read SpeAna 3Band (2.5kHz)
0	0	0	1	1	0	C6H Read SpeAna 3Band (6.3kHz)
0	0	0	1	1	1	C7H Read SpeAna 3Band (16kHz)

■ Write Sequence

In the AK7600, when a “Write-Slave-address assignment” is received at the first byte, the write command at the second byte and data at the third and succeeding bytes are received. At the data block, address and write data are received in a single-byte unit each in accordance with a command code. The number of write data bytes (*1 in Figure 20)is fixed by the received command code.

Usable command codes in write sequence are listed below as “Table 3. List of Usable Command Codes in Write Sequence”.

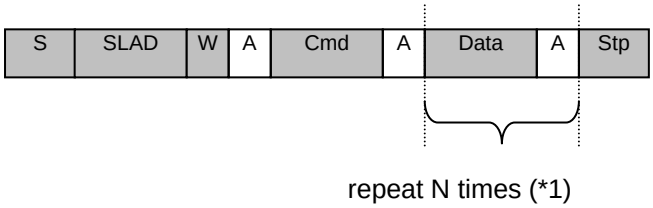


Figure 20. Write Sequence

Command Code	Data Length	Content
40H ~ 4AH	10-byte	16bit coefficient data transferring in 5 coefficient unit or filter unit
80H ~ 89H	20-byte	28bit coefficient data transferring in 5 coefficient unit or filter unit
01H,02H,03H	1byte	Control Register Writing

Table 3. List of Usable Command Codes in Write Sequence

■ Data Format

Data Write

(1)Control Register Write

	SDA
(1) COMMAND	01H, 02H, 03H
(2) DATA	D7~D0

Relationship between COMMAND and control register data.

1) Command 01H is write command for CONT0.
2) Command 02H is write command for CONT1.
3) Command 03H is write command for CONT2.

(2)16bit Coefficient or Delay Data Write

	SDA
(1) COMMAND	40H,41H,42H,43H,44H,45H,46H,47H,48H,49H,4AH
(2) DATA1-1	D15~D8
(3) DATA1-2	D7~D0
(4) DATA2-1	D15~D8
(5) DATA2-2	D7~D0
(6)~(11)	(Continues in 2byte unit to DATA5. In total 10byte DATA)

(3)28bit Coefficient Data Write

	SDA
(1) COMMAND	80H,81H,82H,83H,84H,85H,86H,87H,88H,89H
(2) DATA1-1	0 0 0 0 D27~D24
(3) DATA1-2	D23~D16
(4) DATA1-3	D15~D8
(5) DATA1-4	D7~D0
(6)~(21)	(Continues in 4byte unit to DATA5. In total 20byte DATA)

■ Read Sequence

In the AK7600, when a “write- slave-address assignment” is received at the first byte, the command is send from micro controller in the second byte. When the slave address is received after the start condition, the AK7600 starts outputting the data regarding to command code.

When cancelling read operation before the AK7600 sends all data, assure that a “not acknowledged” signal is received by the AK7600. If this “not acknowledged” signal is not received, the AK7600 continues to send data until specified number, and since it did not release the BUS, the stop condition cannot be properly received.

Usable command codes in read sequence are listed in Table 4

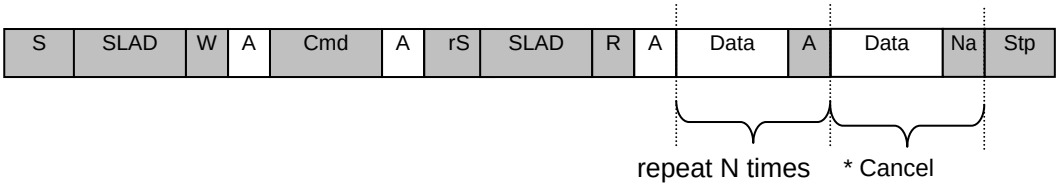


Figure 21. Read Sequence

Command Code	Data Length	Content
40H ~ 4AH	16bit×5	16bit Coefficient; Delay Time Read
80H ~ 89H	32bit×5	28bit Coefficient; Data Read
01H, 02H, 03H	8bit	Control Register Read
C1H, C2H, C3H, C4H, C5H, C6H, C7H	16bit	Spectrum Analyzer Data Read

Table 4. List of Usable Read Command Codes in Read Sequence

Data Read

(1)Control Register Read

	SDA
(1) COMMAND	01H,02H,03H
(2) DATA	D7~D0

Relationship between COMMAND and control register data.

4) Command 01H is read command for CONT0.
5) Command 02H is read command for CONT1.
6) Command 03H is read command for CONT2.

(2)16bit Coefficient or Delay Time Read

	SDA
(1) COMMAND	40H,41H,42H,43H,44H,45H,46H,47H,48H,49H,4AH(Input)
(2) DATA1-1	D15~D8 (Output)
(3) DATA1-2	D7~D0
(4) DATA2-1	D15~D8
(5) DATA2-2	D7~D0
(6)~(11)	(Continues in 2byte unit to DATA5. In total 10byte DATA)

(3)28bit Coefficient Data Read

	SDA
(1) COMMAND	80H,81H,82H,83H,84H,85H,86H,87H,88H,89H (Input)
(2) DATA1-1	0 0 0 0 D27~D24 (Output)
(3) DATA1-2	D23~D16
(4) DATA1-3	D15~D8
(5) DATA1-4	D7~D0
(6)~(21)	(Continues in 4byte unit to DATA5. In total 20byte DATA)

(4) Spectrum Analyzer Data Read

	SDA
(1) COMMAND	C1H, C2H, C3H, C4H, C5H, C6H, C7H (Input)
(2) DATA2	D15 D14 D13 D12 D11 D10 D9 D8 (Output)
(3) DATA1	D7 D6 D5 D4 D3 D2 D1 D0

■ Register Definitions

Register Name: CONT0

	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND (01H)	0	0	0	0	0	0	0	1
Setting bit (1byte)	0	0	0	0	0	PMADC	PMDAC	RSTN
R/W	RD	RD	RD	RD	RD	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	0

RSTN: Internal timing reset
0: Reset (The DZF pin goes to "H" but Register values are not initialized.)
1: Normal Operation

PMDAC: DAC1-3 power management
0: Power Down (All DAC's)
1: Normal Operation

PMADC: ADC power management
0: Power Down
1: Normal Operation

Register Name: CONT1

	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND (02H)	0	0	0	0	0	0	1	0
Setting bit (1byte)	DZD3	DZD2	DZD1	DZLH	DIF	0	0	SMUTE
R/W	R/W	R/W	R/W	R/W	R/W	RD	RD	R/W
Default	0	0	0	0	1	0	0	0

Note) Writing to RD bits is ignored.

DZD3: DZF setting
0: Indicate Zero detect of DAC3 at DZF
1: Ignore Zero detect

DZD2: DZF setting
0: Indicate Zero detect of DAC2 at DZF
1: Ignore Zero detect

DZD1: DZF setting
0: Indicate Zero detect of DAC1 at DZF
1: Ignore Zero detect

DZLH: DZF setting
0: Output "H" as a result of DZF zero detection
1: Output "L" as a result of DZF zero detection

D7	D6	D5	D4	DAC3	DAC2	DAC1	DZF pin output Level
0	0	0	0	Zero	Zero	Zero	H
0	0	1	0	Zero	Zero	-	H
0	1	0	0	Zero	-	Zero	H
0	1	1	0	Zero	-	-	H
1	0	0	0	-	Zero	Zero	H
1	0	1	0	-	Zero	-	H
1	1	0	0	-	-	Zero	H
1	1	1	0	-	-	-	H
0	0	0	1	Zero	Zero	Zero	L
0	0	1	1	Zero	Zero	-	L
0	1	0	1	Zero	-	Zero	L
0	1	1	1	Zero	-	-	L
1	0	0	1	-	Zero	Zero	L
1	0	1	1	-	Zero	-	L
1	1	0	1	-	-	Zero	L
1	1	1	1	-	-	-	L

SMUTE: Soft Mute enable
0: Normal Operation
1: Soft Mute execute for all DAC's

DIF: Digital output format (DIF mode setting)
0: Left justified mode
1: I2S mode (default)

Register Name: CONT2

	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND (03H)	0	0	0	0	0	0	1	1
Setting bit (1byte)	LRCK	BICK	MCKO	Reserved	DO3	DO2	DO1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RD
Default	0	0	0	0	0	0	0	0

LRCK: LRCK output enable
0: LRCK pin outputs "L"
1: Output LRCK(1fs) to the LRCK pin

BICK: BIT clock output enable
0: BICK pin outputs "L"
1: Output BIT clock (64fs) to the BICK pin

MCKO: Master clock output enable
0: CLKO pin outputs "L"
1: Output master clock (256fs) to the CLKO pin

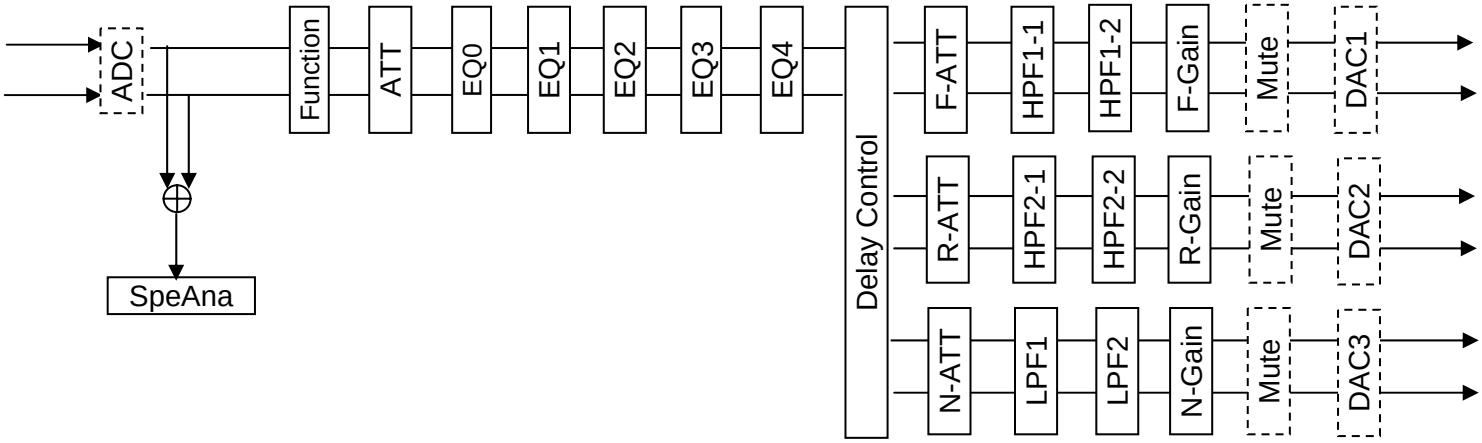
Reserved: Write "0" into this bit.

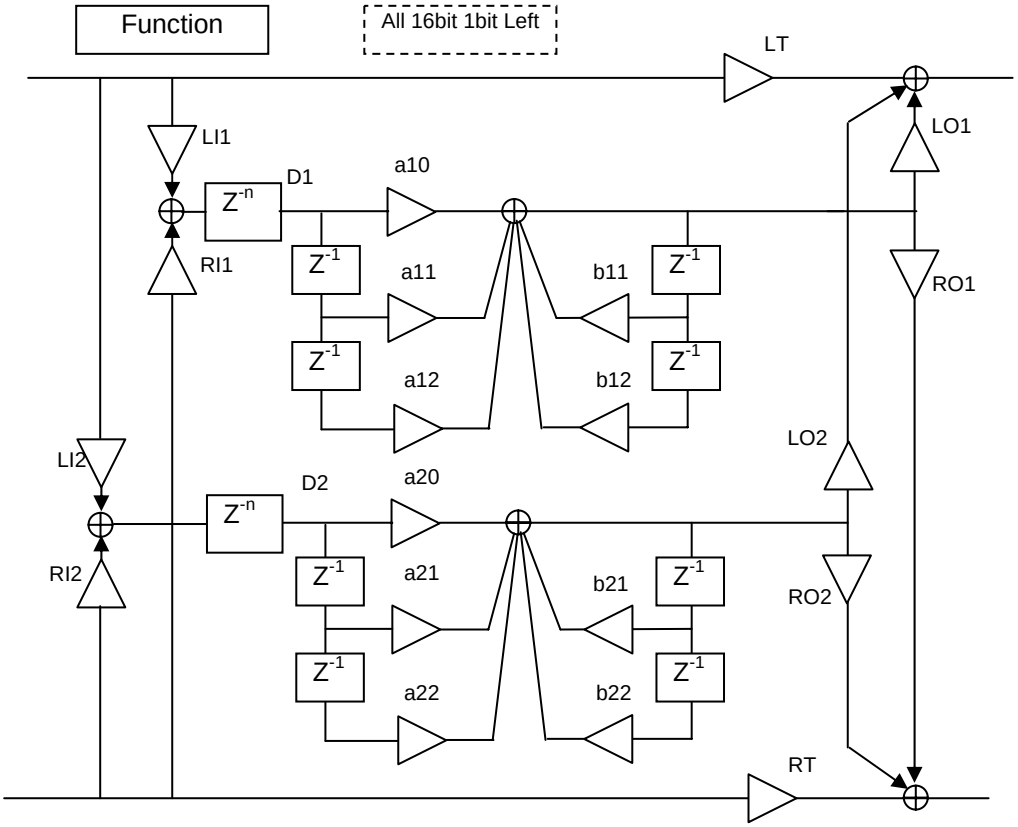
DO3: SDTO3 output enable
0: SDTO3 pin outputs "L"
1: Output audio data to the SDTO3 pin

DO2: SDTO2 output enable
0: SDTO2 pin outputs "L"
1: Output audio data to the SDTO2 pin

DO1: SDTO1 output enable
0: SDTO1 pin outputs "L"
1: Output audio data to the SDTO1 pin

■ **Blocks and Circuits Construction of Command Setting**





Command	40H	Shift Setting	R/W	Default Value
Data 1 (2byte)	LI1 Coefficient	1bit left x2	R/W	0x2000
Data 2 (2byte)	RI1 Coefficient	1bit left x2	R/W	0x2000
Data 3 (2byte)	LT Coefficient	1bit left x2	R/W	0x4000
Data 4 (2byte)	LO1 Coefficient	1bit left x2	R/W	0x0000
Data 5 (2byte)	LO2 Coefficient	1bit left x2	R/W	0x0000

Command	41H	Shift Setting	R/W	Default Value
Data 1 (2byte)	LI2 Coefficient	1bit left x2	R/W	0x2000
Data 2 (2byte)	RI2 Coefficient	1bit left x2	R/W	0x2000
Data 3 (2byte)	RT Coefficient	1bit left x2	R/W	0x4000
Data 4 (2byte)	RO1 Coefficient	1bit left x2	R/W	0x0000
Data 5 (2byte)	RO2 Coefficient	1bit left x2	R/W	0x0000

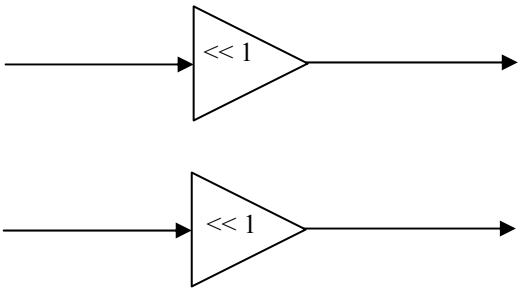
Command	42H	Shift Setting	R/W	Default Value
Data 1 (2byte)	A12 Coefficient	1bit left x2	R/W	0x0000
Data 2 (2byte)	A11 Coefficient	1bit left x2	R/W	0x0000
Data 3 (2byte)	A10 Coefficient	1bit left x2	R/W	0x4000
Data 4 (2byte)	B12 Coefficient	1bit left x2	R/W	0x0000
Data 5 (2byte)	B11 Coefficient	1bit left x2	R/W	0x0000

Command	43H	Shift Setting	R/W	Default Value
Data 1 (2byte)	A22 Coefficient	1bit left x2	R/W	0x0000
Data 2 (2byte)	A21 Coefficient	1bit left x2	R/W	0x0000
Data 3 (2byte)	A20 Coefficient	1bit left x2	R/W	0x4000
Data 4 (2byte)	B22 Coefficient	1bit left x2	R/W	0x0000
Data 5 (2byte)	B21 Coefficient	1bit left x2	R/W	0x0000

Note: All data are R/W.

ATT

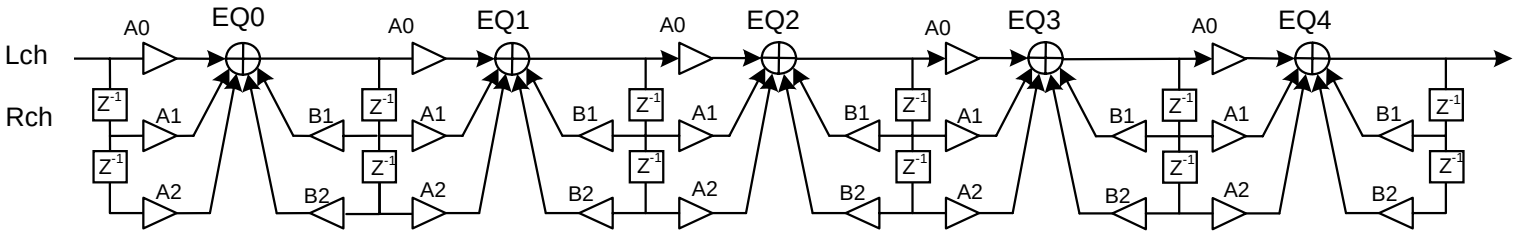
Attenuate input data for both Left and Right channels.



Command	44H	Shift Setting	R/W	Default Value
Data 1 (2byte)	Pre EQ ATT setting coefficient	1bit left x2	R/W	0x4000
Data 2 (2byte)	Dummy	1bit left x2	R/W	0x0000
Data 3 (2byte)	Dummy	1bit left x2	R/W	0x0000
Data 4 (2byte)	Dummy	1bit left x2	R/W	0x0000
Data 5 (2byte)	Dummy	1bit left x2	R/W	0x0000

Note: All data are R/W.

EQ Setting



Command	81H	Shift Setting	R/W	Default Value
Data 1 (4byte)	EQ0 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	EQ0 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	EQ0 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	EQ0 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	EQ0 B1 Coefficient	1bit left x 2	R/W	0x00000000

Command	82H	Shift Setting	R/W	Default Value
Data 1 (4byte)	EQ1 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	EQ1 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	EQ1 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	EQ1 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	EQ1 B1 Coefficient	1bit left x 2	R/W	0x00000000

Command	83H	Shift Setting	R/W	Default Value
Data 1 (4byte)	EQ2 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	EQ2 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	EQ2 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	EQ2 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	EQ2 B1 Coefficient	1bit left x 2	R/W	0x00000000

Note: All data are R/W.

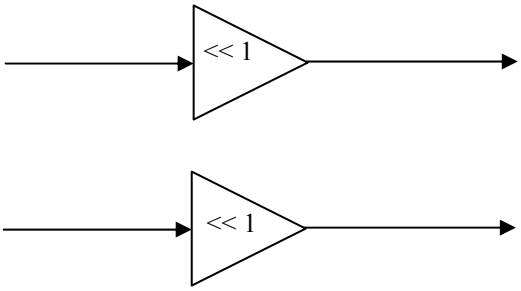
Command	45H	Shift Setting	R/W	Default Value
Data 1 (2byte)	EQ3 A2 Coefficient	1bit left x2	R/W	0x0000
Data 2 (2byte)	EQ3 A1 Coefficient	1bit left x2	R/W	0x0000
Data 3 (2byte)	EQ3 A0 Coefficient	1bit left x2	R/W	0x4000
Data 4 (2byte)	EQ3 B2 Coefficient	1bit left x2	R/W	0x0000
Data 5 (2byte)	EQ3 B1 Coefficient	1bit left x2	R/W	0x0000

Command	46H	Shift Setting	R/W	Default Value
Data 1 (2byte)	EQ4 A2 Coefficient	1bit left x2	R/W	0x0000
Data 2 (2byte)	EQ4 A1 Coefficient	1bit left x2	R/W	0x0000
Data 3 (2byte)	EQ4 A0 Coefficient	2bit left x4	R/W	0x2000
Data 4 (2byte)	EQ4 B2 Coefficient	1bit left x2	R/W	0x0000
Data 5 (2byte)	EQ4 B1 Coefficient	1bit left x2	R/W	0x0000

Note: All data are R/W.

F-ATT, R-ATT, N-ATT

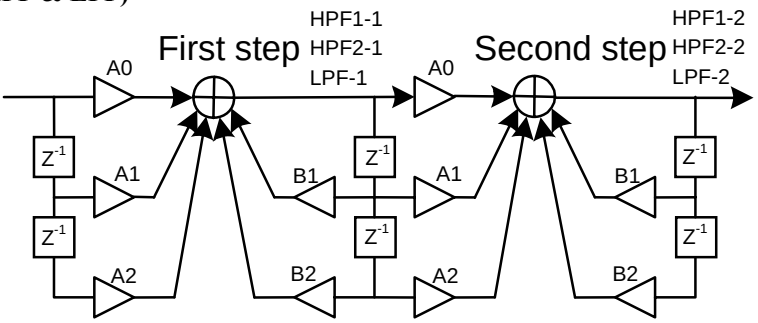
Amplify or regulate each Front (L1, R1), Rear (L2, R2) and SW (L3, R3) X'Over filter input data.



Command	47H	Shift Setting	R/W	Default Value
Data 1 (2byte)	Front ATT setting coefficient	1bit left x2	R/W	0x4000
Data 2 (2byte)	Rear ATT setting coefficient	1bit left x2	R/W	0x4000
Data 3 (2byte)	SW(NF) ATT setting coefficient	1bit left x2	R/W	0x4000
Data 4 (2byte)	Dummy	1bit left x2	R/W	0x0000
Data 5 (2byte)	Dummy	1bit left x2	R/W	0x0000

Note: All data are R/W.

X'Over filter (HPF & LPF)



Command	84H	Shift Setting	R/W	Default Value
Data 1 (4byte)	HPF1-1 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	HPF1-1 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	HPF1-1 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	HPF1-1 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	HPF1-1 B1 Coefficient	1bit left x 2	R/W	0x00000000

Note: All data are R/W.

Command	85H	Shift Setting	R/W	Default Value
Data 1 (4byte)	HPF1-2 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	HPF1-2 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	HPF1-2 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	HPF1-2 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	HPF1-2 B1 Coefficient	1bit left x 2	R/W	0x00000000

Command	86H	Shift Setting	R/W	Default Value
Data 1 (4byte)	HPF2-1 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	HPF2-1 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	HPF2-1 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	HPF2-1 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	HPF2-1 B1 Coefficient	1bit left x 2	R/W	0x00000000

Command	87H	Shift Setting	R/W	Default Value
Data 1 (4byte)	HPF2-2 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	HPF2-2 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	HPF2-2 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	HPF2-2 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	HPF2-2 B1 Coefficient	1bit left x 2	R/W	0x00000000

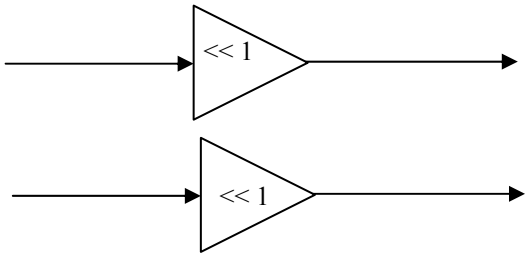
Command	88H	Shift Setting	R/W	Default Value
Data 1 (4byte)	LPF-1 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	LPF-1 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	LPF-1 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	LPF-1 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	LPF-1 B1 Coefficient	1bit left x 2	R/W	0x00000000

Command	89H	Shift Setting	R/W	Default Value
Data 1 (4byte)	LPF-2 A2 Coefficient	1bit left x 2	R/W	0x00000000
Data 2 (4byte)	LPF-2 A1 Coefficient	1bit left x 2	R/W	0x00000000
Data 3 (4byte)	LPF-2 A0 Coefficient	1bit left x 2	R/W	0x04000000
Data 4 (4byte)	LPF-2 B2 Coefficient	1bit left x 2	R/W	0x00000000
Data 5 (4byte)	LPF-2 B1 Coefficient	1bit left x 2	R/W	0x00000000

Note: All data are R/W.

F-Gain, R-Gain, N-Gain

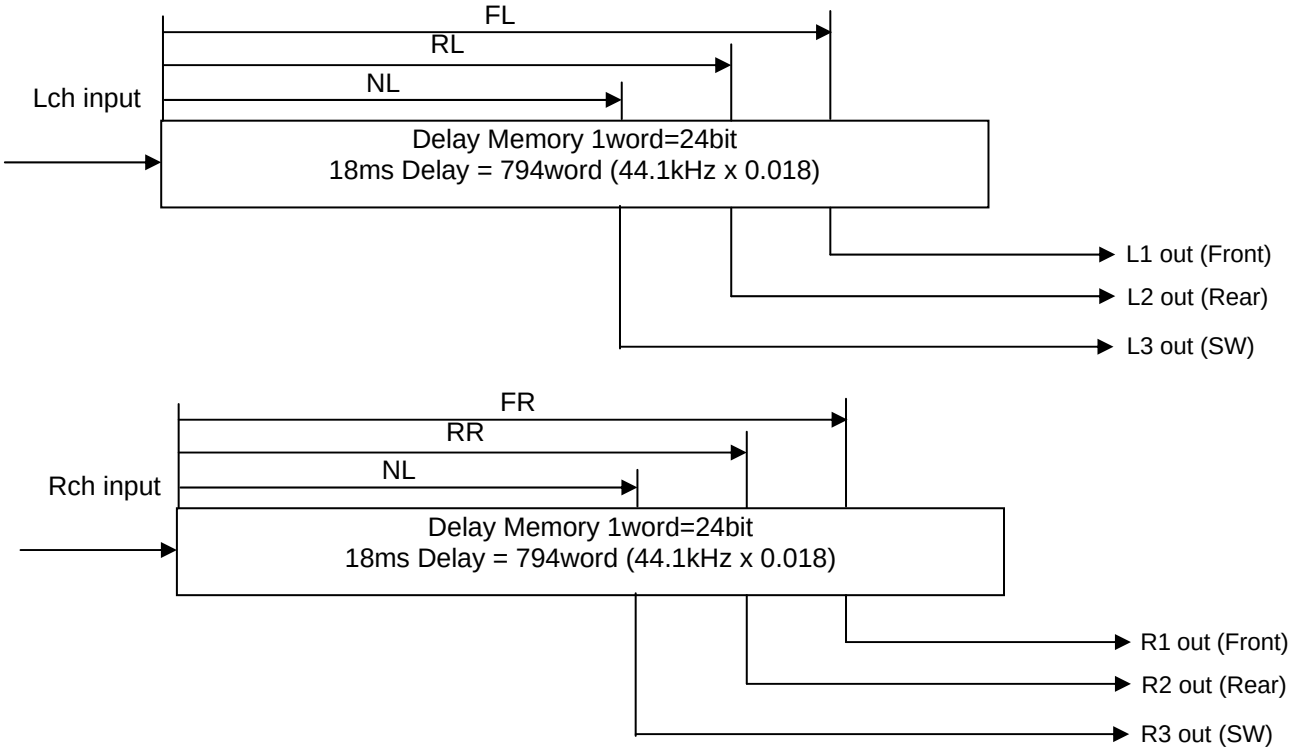
Amplify or regulate each Front (L1, R1), Rear (L2, R2) and SW (L3, R3) X'Over filter output data.



Command	48H	Shift Setting	R/W	Default Value
Data 1 (2byte)	Front Gain setting coefficient	1bit left x 2	R/W	0x4000
Data 2 (2byte)	Rear Gain setting coefficient	1bit left x 2	R/W	0x4000
Data 3 (2byte)	SW(NF) Gain setting coefficient	1bit left x 2	R/W	0x4000
Data 4 (2byte)	Dummy	1bit left x 2	R/W	0x0000
Data 5 (2byte)	Dummy	1bit left x 2	R/W	0x0000

■ Delay Time Setting (fs step)

1. D1 or D2 delay time setting of Function2
2. Delay time setting of each FL, FR, RR, RL, NL and NR channel



(1/fs = 1/44100 = approximately 0.0226ms)= one unit.

Command	49H	Setting Unit	R/W	Default Value
Data 1 (2byte)	Function2 D1 delay time Set range (0x0000~0x002D)	Delay time: 1/fs unit	R/W	0x0000
Data 2 (2byte)	Front L1 out delay time Set range (0x0000~0x031A)	Delay time: 1/fs unit	R/W	0x0000
Data 3 (2byte)	Rear L2 out delay time Set range (0x0000~0x031A)	Delay time: 1/fs unit	R/W	0x0000
Data 4 (2byte)	SW L3 out delay time Set range (0x0000~0x031A)	Delay time: 1/fs unit	R/W	0x0000
Data 5 (2byte)	Dummy	-	R/W	0x0000

Command	4AH	Setting Unit	R/W	Default Value
Data 1 (2byte)	Function2 D2 delay time Set range (0x0000~0x002D)	Delay time: 1/fs unit	R/W	0x0000
Data 2 (2byte)	Front R1 out delay time Set range (0x0000~0x031A)	Delay time: 1/fs unit	R/W	0x0000
Data 3 (2byte)	Rear R2 out delay time Set range (0x0000~0x031A)	Delay time: 1/fs unit	R/W	0x0000
Data 4 (2byte)	SW R3 out delay time Set range (0x0000~0x031A)	Delay time: 1/fs unit	R/W	0x0000
Data 5 (2byte)	Dummy	-	R/W	0x0000

Note: All data are R/W.
When the delay time is set over its limit, it will be set to the maximum value.

Spectrum Analyzer

Each data level read of Spectrum Analyzer

Command	C1H	R/W
Data1 (2byte)	68Hz Level	RD

Command	C1H	R/W
Data1 (2byte)	160Hz Level	RD

Command	C1H	R/W
Data1 (2byte)	400Hz Level	RD

Command	C1H	R/W
Data1 (2byte)	1kHz Level	RD

Command	C1H	R/W
Data1 (2byte)	2.5kHz Level	RD

Command	C1H	R/W
Data1 (2byte)	6.3kHz Level	RD

Command	C1H	R/W
Data1 (2byte)	16kHz Level	RD

Measuring Frequency of Spectrum Analyzer

There are 7 bands of the detection frequency of spectrum analyzer level at Fs=44.1kHz.

Band	1	2	3	4	5	6	7
f0[Hz]	68	160	400	1000	2500	6300	16000

SYSTEM DESIGN

Figure 22 shows the system connection diagram. An evaluation board (AKD7600) is available for fast evaluation as well as suggestions for peripheral circuitry.

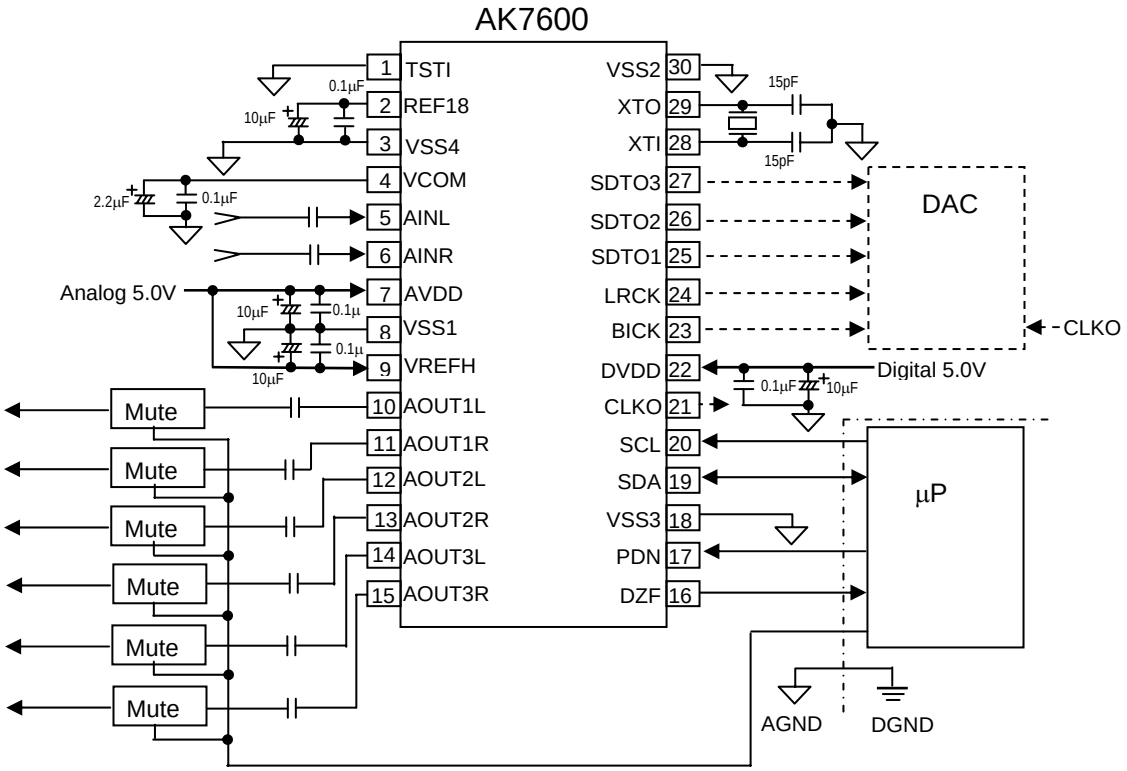


Figure 22. Typical Connection Diagram

Note: Do not take load current from the REF18 pin.

1. Grounding and Power Supply Decoupling

The AK7600 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from the system's analog supply. If AVDD and DVDD are supplied separately, the power-up sequence is not critical. **VSS1, VSS2, VSS3 and VSS4 of the AK7600 should be connected to the analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK7600 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The input voltage to the VREFH pin sets the analog output range. Usually the VREFH pin is connected to AVDD and a 0.1μF ceramic capacitor is connected between AVDD and VSS1. VCOM is a signal ground of this chip (AVDD/2). The electrolytic capacitor around 2.2μF attached between VCOM anVSS1 eliminates the effects of high frequency noise. The ceramic capacitor in particular should be connected as close as possible to the pin. No load current may be taken from the VCOM pin. All signals, especially clock, should be kept away from VREFH and VCOM in order to avoid unwanted coupling into the AK7600.

3. Analog Inputs

The ADC inputs is single-ended and biased to VCOM voltage (AVDD/2) internally by 45kΩ(typ). The inputs signal range scales with nominally at 0.65 x VREFH Vpp (typ)@fs=44.1kHz. The AK7600 can accept input voltage from VSS1 to AVDD. The output code format is 2's complement. Input DC offset is canceled by an integrated high-pass filter.

The AK7600 samples the analog input at 64fs(@fs=44.1kHz). A digital filter removes the noise over the stopband attenuation level, except for a band of integral multiplication of 64fs. AK7600 has an integrated anti-alias RC filter in order to reduce the noise at 64fs.

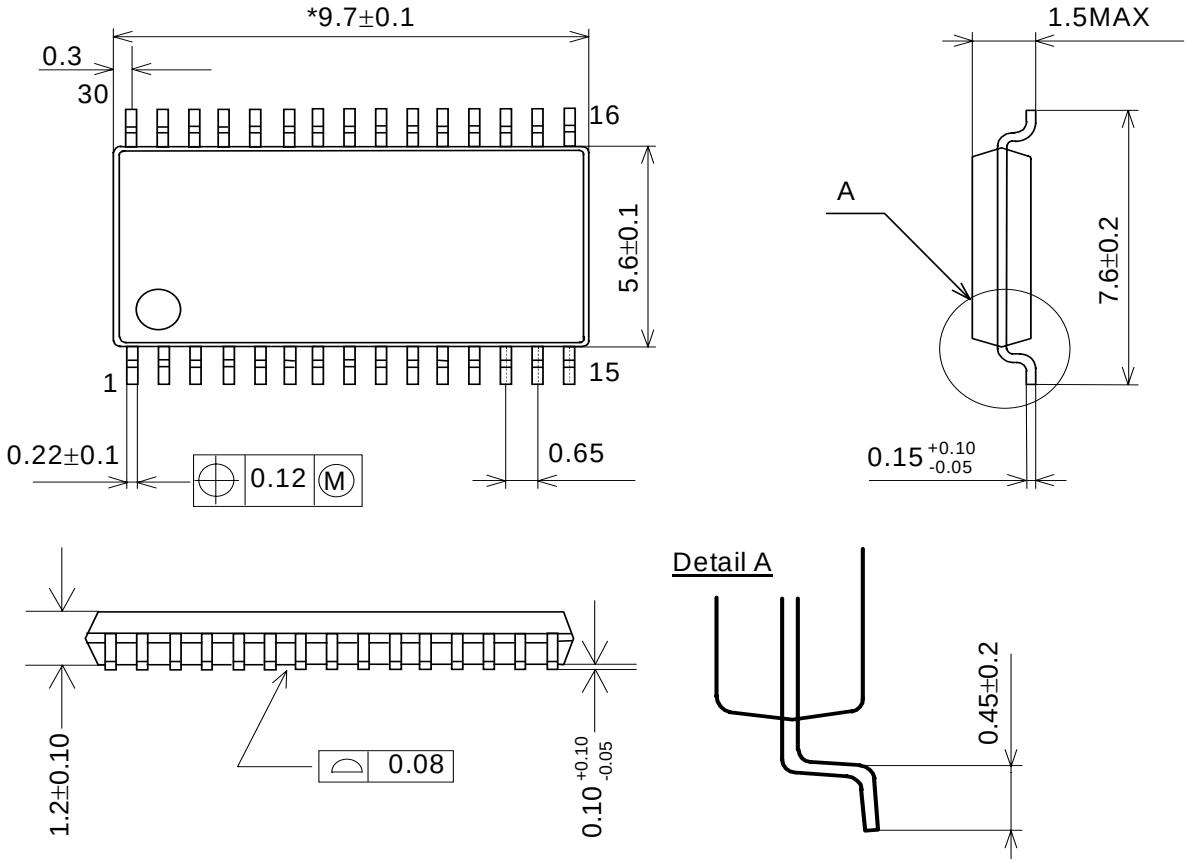
4. Analog output

The DAC output is single-ended and output range is 0.65xVREFH Vpp (typ) centered on VCOM. The bias voltage of the external summing circuit is supplied externally. The input data format is two's compliment. Positive full-scale output corresponds to 7FFFFFH (@24bit) input code, Negative full scale is 800000H (@24bit) and VCOM voltage ideally is 000000H (@24bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an integrated switched capacitor filter (SCF) and a continuous time filter (CTF).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs has DC offset of VCOM.

PACKAGE

30pin VSOP (Unit: mm)

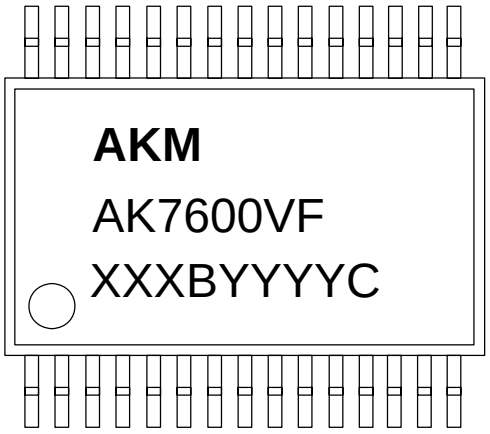


NOTE: Dimension "*" does not include mold flash.

■ Materials and Lead Specification

Package: Epoxy
Lead frame: Copper
Lead-finish: Soldering plate (Pb free)

MARKING



XXXBYYYYC Date code identifier

XXXB: Lot number (X: Digit number, B: Alpha character)
YYYYC: Assembly date (Y: Digit number, C: Alpha character)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/09/03	00	First Edition		