

## LC75384NE-R, 75384NW

## Electronic Volume and Tone Control for Car Stereo Systems



## Overview

The LC75384NE-R and LC75384NW are electronic volume and tone control ICs that can implement volume, balance, fader, bass/treble/mid, loudness, input switching, and input gain control functions with a minimum number of external components.

## **Features**

• Volume: 81 positions: from 0 dB to -79 dB in 1-dB steps and  $-\infty$ .

A balance function can be implemented by controlling the left and right volume settings independently.

- Fader: Either the rear or front outputs can be attenuated over 16 positions. (16 positions: From 0 dB to -2 dB in 1-dB steps, from -2 dB to -20 dB in 2-dB steps, from -20 to -30 dB in one 10-dB step, -45 dB, -60 dB, and -∞.)
- Bass/treble/mid: Control over ±12 dB in 2-dB steps in each band.
- Input gain: The input signal can be amplified by from 0 dB to +18.75 dB in 1.25-dB steps.

- Input switching: The left and right channels can each be selected from one of 5 inputs. (Four are single-ended inputs and one is a differential input.)
- Loudness: Taps are output from a 2-dB step volume control ladder resistor starting at the -32-dB position. A loudness function can be implemented by attaching external capacitors and resistors.
- On-chip buffer amplifiers minimize the number of required external components.
- Minimal switching noise when no input signals are present due to fabrication in a silicon gate CMOS process that minimizes the noise generated by internal switches.
- Use of zero-cross switching circuits for internal switches minimizes switching noise when signals are present.
- Built-in  $V_{DD}/2$  reference voltage generator circuit
- All controls can be set from serial input data.

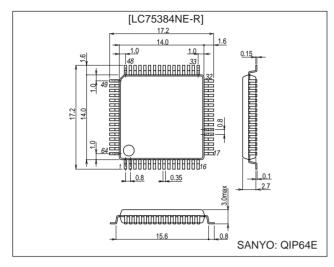
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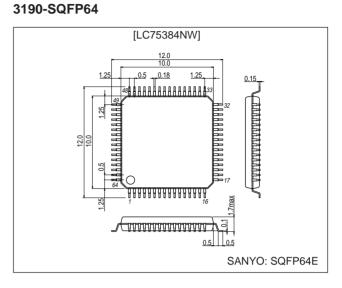
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## **Package Dimensions**

unit: mm

#### 3159-QIP64E





# Specifications Absolute Maximum Ratings at Ta = 25°C, $V_{\rm SS}$ = 0 V

Parameter	Symbol	Conditions	Ratings	Unit	
Maximum supply voltage	$V_{\text{DD}}$ max	V <sub>DD</sub> max V <sub>DD</sub>		11	V
Maximum input voltage	V <sub>IN</sub> max	All input pins	All input pins		
Allowable newer dissinction	Pd max	Ta $\leq$ 85°C, when mounted on a printed	LC75384NE-R	500	mW
Allowable power dissipation	Pumax	circuit board	LC75384NW	420	mvv
Operating temperature	Topr		-40 to +85	°C	
Storage temperature	Tstg		-50 to +125	°C	

#### Allowable Operating Ranges at $Ta = 25^{\circ}C$ , $V_{ss} = 0 V$

Parameter	Sumbol	Conditions		Unit		
Parameter	Symbol			typ	max	Unit
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	6.0		10.5	V
Input high-level voltage	VIH	CL, DI, CE, MUTE	4.0		V <sub>DD</sub>	V
Input low-level voltage	VIL	CL, DI, CE, MUTE	V <sub>SS</sub>		1.0	V
Input voltage amplitude	V <sub>IN</sub>		V <sub>ss</sub>		V <sub>DD</sub>	Vр-р
Input pulse width	t <sub>øW</sub>	CL	1			μs
Setup time	t <sub>setup</sub>	CL, DI, CE	1			μs
Hold time	thold	CL, DI, CE	1			μs
Operating frequency	fopg	CL			500	kHz

## Electrical Characteristics at Ta = 25°C, $V_{\text{DD}}$ = 9 V, $V_{\text{SS}}$ = 0 V

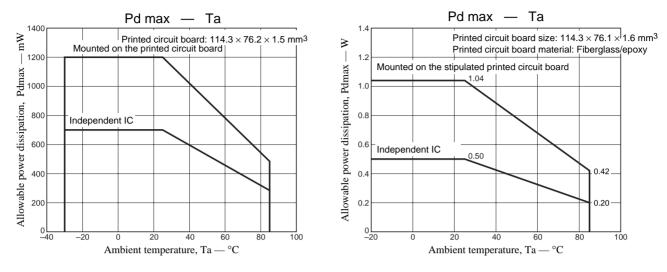
Parameter	Cumbal	Pins	Conditions		Ratings			
Parameter	Symbol Pins		Conditions	min	typ	max	- Unit	
[Input Block]								
Input resistance	Rin	L1 to L4, R1 to R4		30	50	70	kΩ	
Minimum input gain	Ginmin	L1 to L4, R1 to R4		-1	0	+1	dB	
Maximum input gain	Ginmax			+16.5	+18.75	+21	dB	
Inter-step setting error	ATerr					±0.6	dB	
Left/right balance	BAL					±0.5	dB	
[Volume Block]	·							
Input resistance	Rvr	LVRIN, RVRIN, loudness off		113	226	339	kΩ	
Inter-step setting error	ATerr					±0.5	dB	
Left/right balance	BAL					±0.5	dB	
[Tone Control Block]	·							
Inter-step setting error	ATerr					±1.0	dB	
Bass control range	Gbass		max. boost/cut	±9	±12	±15	dB	
Mid control range	Gmid		max. boost/cut	±9	±12	±15	dB	
Treble control range	Gtre		max. boost/cut	±9	±12	±15	dB	
Left/right balance	BAL					±0.5	dB	
[Fader Block]	·							
Input resistance	Rfed	LFIN, RFIN		25	50	100	kΩ	
			0 dB to –2 dB			±0.5	dB	
Inter aton potting arror	ATerr		-2 dB to -20 dB			±1	dB	
Inter-step setting error	ATER		-20 dB to -30 dB			±2	dB	
			–30 dB to –60 dB			±3	dB	
Left/right balance	BAL					±0.5	dB	

### **Overall Characteristics**

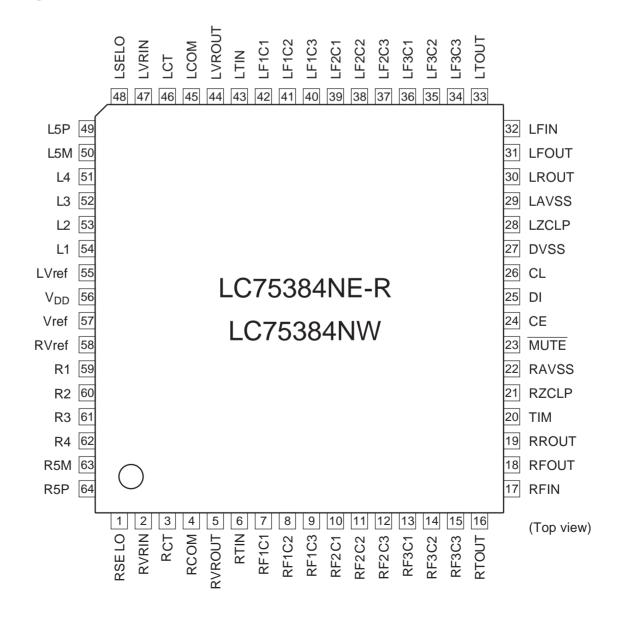
Parameter	Cumhal	Conditions		Ratings		Unit	
Parameter	Symbol	Conditions		typ	max		
Total harmonic distortion	THD 1	$V_{IN} = -10 \text{ dBV}, \text{ f} = 1 \text{ kHz}$		0.004		%	
	THD 2	$V_{IN} = -10 \text{ dBV}, \text{ f} = 10 \text{ kHz}$		0.006		%	
Inter-input crosstalk	СТ	V <sub>IN</sub> = 1 Vrms, f = 1 kHz	80	88		dB	
Left/right channel crosstalk	СТ	V <sub>IN</sub> = 1 Vrms, f = 1 kHz	80	88		dB	
Maximum attenuation	V <sub>o</sub> min 1	V <sub>IN</sub> = 1 Vrms, f = 1 kHz	80	88		dB	
Maximum altenuation	V <sub>o</sub> min 2	$V_{\text{IN}}$ = 1 Vrms, f = 1 kHz, INMUTE, with the fader set to $-\infty$	90	95		dB	
	V <sub>N</sub> 1	All controls flat, with the IHF-A filter		5	10	μV	
Output noise voltage	V <sub>N</sub> 2	All controls flat, with a 20 Hz to 20 kHz bandpass filter		7	15	μV	
Current drain	I <sub>DD</sub>			33	40	mA	
Input high-level current	IIH	CL, DI, CE, V <sub>IN</sub> = 9 V			10	μA	
Input low-level current	IIL	CL, DI, CE, $V_{IN} = 0 V$	-10			μA	
Maximum input voltage	V <sub>CL</sub>	THD = 1 %, $R_L$ = 10 k $\Omega$ , all controls flat, $f_{IN}$ = 1 kHz	2.5	2.9		Vrms	
Common-mode rejection ratio	CMRR	V <sub>IN</sub> = 0 dBV, f = 1 kHz	45			dB	

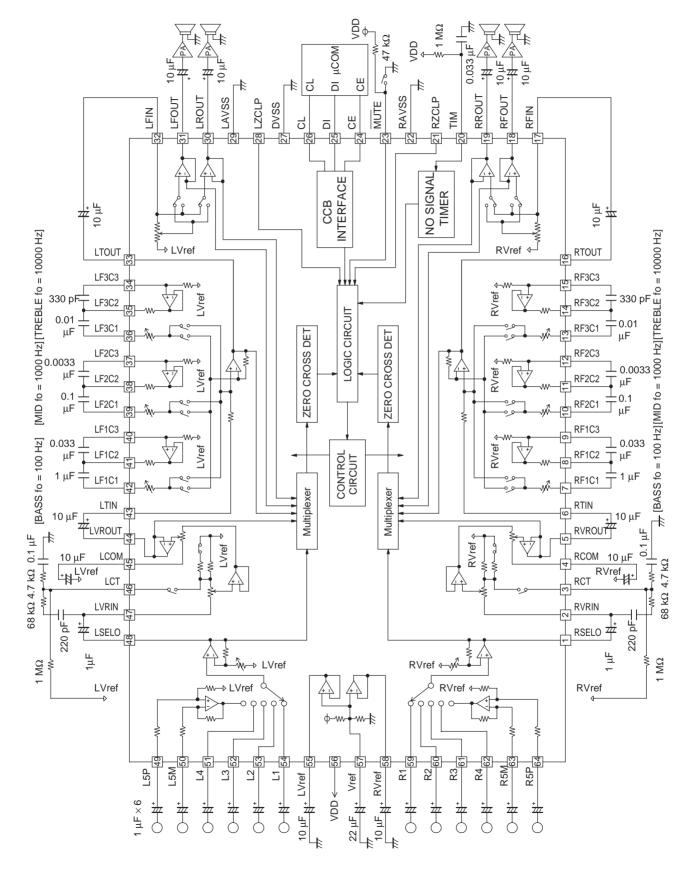
#### [LC75384NE-R]

[LC75384NW]



#### **Pin Assignment**





#### Equivalent Circuit and Sample Application Circuit Diagram

• In the LC75384NW version, LZCLP (pin 28) and RZCLP (pin 21) are unused, and must be left open.

#### **Pin Functions**

Pin No.	Pin	Function	Notes
54	L1		
53	L2		↓ V DD
52	L3		
51	L4		
59	R1	Single end inputs	
60	R1 R2		7777
61	R3		LVref RVref
62	R4		RVIEI
50 49 63 64	L5M L5P R5M R5P	• Differential inputs	P ↓ VDD W ↓ VDD P ↓ VDD LVref RVref
48 1	LSEL0 RSEL0	Input selector outputs	VDD
47 2	LVRIN RVRIN	<ul> <li>Inputs for the 2-dB step volume control</li> <li>These inputs must be driven from low-impedance circuits.</li> </ul>	LVref RVref
46 3	LCT RCT	• Loudness function pins. Connect the high-band compensation RC circuits between the LCT (RCT) and the LVRIN (RVRIN) pins and connect the low-band compensation RC circuits between the LCT (RCT) and LVREF (RVREF).	
45 4	LCOM RCOM	<ul> <li>2-dB step volume control outputs</li> <li>To reduce switching noise, each of these pins should be connected to LVREF (RVREF) through a capacitor.</li> </ul>	→ V <sub>DD</sub> → → → → → → → → → → → → → → → → → → →
44 5	LVROUT RVROUT	• Output from the 1-dB step volume control	V <sub>DD</sub>

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Pin No.	Pin	Function	Equivalent circuit
			Υ V <sub>DD</sub>
43	LTIN	Equalizer input	
6	RTIN		
			<sup>///</sup> LVref
			RVref
42	LF1C1	Connections for the capacitors for the equalizer's F1 band	
41	LF1C2	filter.	
40	LF1C3	The low band compensation capacitors must be connected	
7	RF1C1	between the following pins:	
8	RF1C2	LF1C1 (RF1C1) and LF1C2 (RF1C2)	C2
9	RF1C3	LF1C2 (RF1C2) and LF1C3 (RF1C3)	
39	LF2C1	Connections for the capacitors for the equalizer's F2 band	A Contraction of the second se
38	LF2C2	filter.	6
37	LF2C3	The low band compensation capacitors must be connected	LVref
10	RF2C1	between the following pins:	RVref
11	RF2C2	LF2C1 (RF2C1) and LF2C2 (RF2C2)	γ V <sub>DD</sub>
12	RF2C3	LF2C2 (RF2C2) and LF2C3 (RF2C3)	עטיע
36	LF3C1	Connections for the capacitors for the equalizer's F3 band	C1 [
35	LF3C2	filter.	
34	LF3C3	The low band compensation capacitors must be connected	777
13	RF3C1	between the following pins:	
14	RF3C2	LF3C1 (RF3C1) and LF3C2 (RF3C2)	
15	RF3C3	LF3C2 (RF3C2) and LF3C3 (RF3C3)	
33 16	LTOUT RTOUT	• Equalizer output	
32 17	LFIN RFIN	<ul> <li>Fader block inputs</li> <li>These inputs must be driven from low-impedance circuits.</li> </ul>	
			° ∧DD
31	LFOUT	Fader block outputs. The front and rear outputs can be	
30	LROUT	attenuated independently. The attenuation is the same in	
18	RFOUT	the left and right channels.	
19	RROUT		777
57	Vref	• $V_{DD}/2$ voltage generator block. A capacitor with a value of about 10 $\mu$ F must be inserted between Vref and AV <sub>SS</sub> (V <sub>SS</sub> ) to reduce power supply ripple.	V <sub>DD</sub>
55	LVref	Internal analog system ground     These pips must be bandled as shown in the sample	
58	RVref	These pins must be handled as shown in the sample application circuit.	LVref 777
			RVref

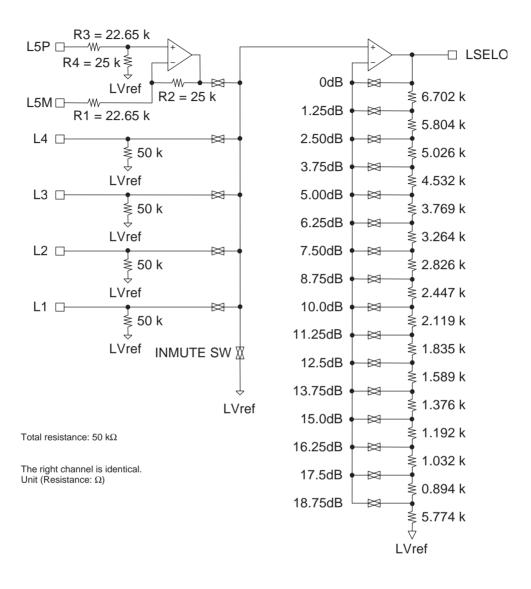
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Pin No.	Pin	Function	Equivalent circuit
56	V <sub>DD</sub>	Power supply	
27	DV <sub>SS</sub>	Logic system ground	
29 22	LAV <sub>SS</sub> RAV <sub>SS</sub>	Analog system ground	
28 21	LZCLP RZCLP	<ul> <li>Band limiting for the zero cross detection circuit</li> <li>These pins are normally left open.</li> <li>These pins are unused in the LC75384NW version and must be left open.</li> </ul>	LC75384NE-R VDD LVref RVref
23	MUTE	<ul> <li>External muting control</li> <li>When this pin is set to the V<sub>SS</sub> level, the fader volume block is forcibly set to -∞.</li> </ul>	
20	TIM	<ul> <li>Used for the zero cross circuit no-signal timer function.</li> <li>If a zero cross signal does not occur between the point when data is loaded and the point when the timer times out, the data will be stored forcibly when the timer times out.</li> </ul>	
26	CL	Serial data and clock inputs used for device control	
25	DI		
24	CE	<ul> <li>Chip enable input. Data is written to the internal latch when this pin goes from high to low. The analog switches then operate.</li> <li>Data transfers are enabled when this pin is high.</li> </ul>	

#### **Internal Equivalent Circuits**

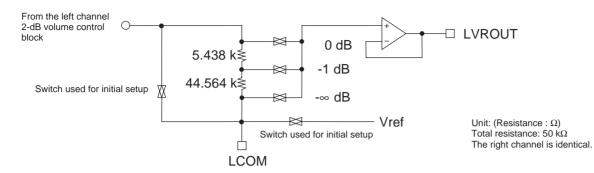
#### Selector Block Equivalent Circuit



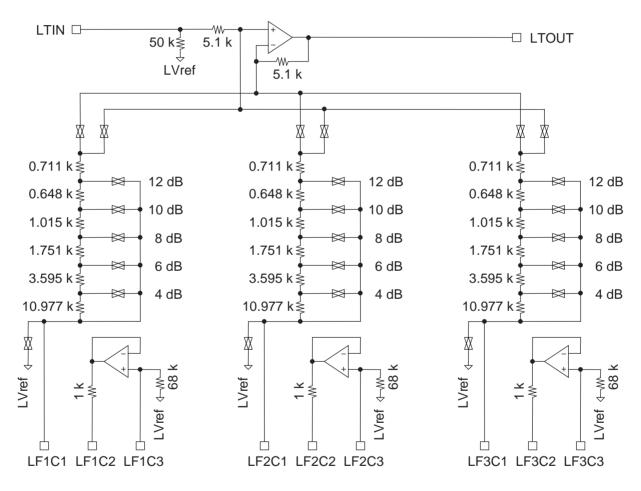
2-dB Step Volume Control Block Equivalent Circuit

		0dB	To the left
	41.139 k 🏅	-2dB	channel 1-dB step block
	32.678 k 🛓	-4dB	
	25.957 k ≩	-6dB	
	20.618 k 🛓		
	16.378 k 🕏	-8dB	
• The total resistance above the	13.009 k 🕏	-10dB	
tap is 195 kΩ	10.334 k 🕏	-12dB	
	8.208 k ≹	-14dB	
	6.520 k ≶	-16dB	
	5.179 k 📚	-18dB	
	4.114 k 📚	-20dB	
	3.268 k ≷	-22dB	
	2.596 k ≩	-24dB	
	2.062 k ≷	-26dB	
	•	-28dB	
	1.638 k ≶	-30dB	
	1.301 k ≰	-32dB	The right channel is identi Unit (Resistance: Ω)
	6.344 k ≰	-34dB	· · · · ·
	5.040 k 養	-36dB	
5.750 k≸	4.003 k ≸	-38dB	
	3.180 k ≸	-40dB	
$\mathbf{x}$	2.526 k ≹	-42dB	
	2.006 k 💈	-44dB	
	1.594 k ≸	-46dB	
The total resistance below	1.266 k 💈	-48dB	
the tap is 30.847 k $\Omega$	1.006 k 🛓	-50dB	
	0.799 k 퇒		
	0.634 k 🕏	-52dB	
	0.504 k 🛓	-54dB	
	0.400 k 🕏	-56dB	
	0.318 k 🐓	-58dB	
	0.253 k ≨	-60dB	
	0.201 k ≩	-62dB	
	0.159 k ≩	-64dB	
	0.127 k ≩	-66dB	
	0.101 k ≩	-68dB	
	•	-70dB	
	0.080 k ≰	-72dB	
	0.063 k ≸	-74dB	
	0.050 k ≸	-76dB	
	0.040 k 📚	-78dB	
	0.154 k ≶	-∞ dB	
	$\checkmark$		

1-dB Step Volume Control Block Equivalent Circuit



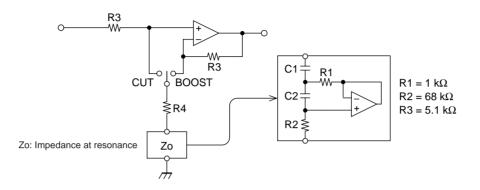
Three-Band Graphic Equalizer Block Equivalent Circuit Diagram



Unit: (Resistance : Ω)

The external capacitors C1 and C2 used with the LC75384W form the structural element of the simulated inductor implemented by the IC. This section present the equivalent circuit and the method for calculating the constants required to obtain the desired center frequency.

(A) Simulated inductor equivalent circuit



#### (B) Calculation

Specifications: 1. Center frequency:  $F_0 = 100 \text{ Hz}$ 

2. Q at maximum boost:  $Q_{+12dB} = 0.9$ 

1. Determine the sharpness,  $Q_0$ , of the simulated inductor itself.

$$Q0 = \frac{(R1 + R4)}{R1} \times Q_{+12dB} \approx 1.5399$$

2. Determine C1.

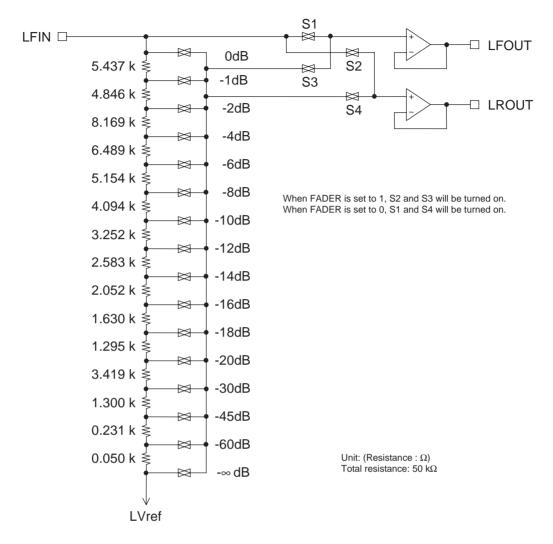
$$C1 = 1/2\pi F_0 R 1 Q_0 \neq 1 \ (\mu F)$$

3. Determine C2.

 $C2 = Q_0/2\pi F_0 R2 \neq 0.036 \ (\mu F)$ 

Note: \* See the equivalent circuit diagram for the tone control block on page 11 for details on the internal resistor.

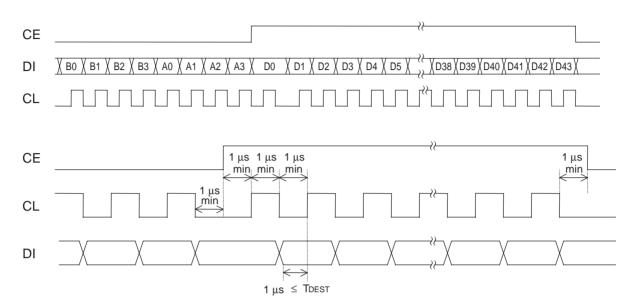
Fader Volume Control Block Equivalent Circuit



If data that sets the main volume control 1-dB step circuit to  $-\infty$  is sent to the device, switches S1 and S2 will be opened (off) and switches S3 and S4 will be closed (on).

#### **Control System Timing and Data Format**

The LC75384NE-R/NW are controlled by applying the stipulated data to the CL, DI, and CE pins. The data consists of a total of 52 bits, of which 8 bits are the device address and 44 bits are the actual control data.



#### • Address code (B0 to A3)

The LC75384NE-R/NW have an 8-bit address codes, and can be used along with other ICs that support the Sanyo CCB serial bus.

Address code

(LSB)	B0	B1	B2	B3	A0	A1	A2	A3	(81HEX)
	1	0	0	0	0	0	0	1	

• Control code allocation

Input switching control

D0	D1	D2	Setting					
0	0	0	L1 (R1)					
1	0	0	L2 (R2)					
0	1	0	L3 (R3)					
1	1	0	L4 (R4)					
0	0	1	L5 (R5)					
0	1	1		IC test values. These values must not				
1	1	1		be used during normal operation.				

D3 IC test bit. This bit must be set to 0 during normal operation.

#### Input gain control

D4	D5	D6	D7	Operation	
0	0	0	0	0 dB	
1	0	0	0	+1.25 dB	
0	1	0	0	+2.50 dB	
1	1	0	0	+3.75 dB	
0	0	1	0	+5.00 dB	
1	0	1	0	+6.25 dB	
0	1	1	0	+7.50 dB	
1	1	1	0	+8.75 dB	
0	0	0	1	+10.0 dB	
1	0	0	1	+11.25 dB	
0	1	0	1	+12.5 dB	
1	1	0	1	+13.75 dB	
0	0	1	1	+15.0 dB	
1	0	1	1	+16.25 dB	
0	1	1	1	+17.5 dB	
1	1	1	1	+18.75 dB	

#### Volume Control

D8	D9	D10	D11	D12	D13	D14	D15	Operation
								1-dB step
0								0 dB
1								–1 dB
		2-dB step						
	0	0	0	0	0	0	0	0 dB
	1	0	0	0	0	0	0	–2 dB
	0	1	0	0	0	0	0	–4 dB
	1	1	0	0	0	0	0	–6 dB
	0	0	1	0	0	0	0	8 dB
	1	0	1	0	0	0	0	-10 dB
	0	1	1	0	0	0	0	–12 dB
	1	1	1	0	0	0	0	-14 dB
	0	0	0	1	0	0	0	-16 dB
	1	0	0	1	0	0	0	–18 dB
	0	1	0	1	0	0	0	-20 dB
	1	1	0	1	0	0	0	-22 dB
	0	0	1	1	0	0	0	-24 dB -26 dB
	0	1	1	1	0	0	0	-28 dB
	1	1	1	1	0	0	0	-30 dB
	0	0	0	0	1	0	0	-32 dB
	1	0	0	0	1	0	0	-34 dB
	0	1	0	0	1	0	0	-36 dB
	1	1	0	0	1	0	0	–38 dB
	0	0	1	0	1	0	0	-40 dB
	1	0	1	0	1	0	0	–42 dB
	0	1	1	0	1	0	0	–44 dB
	1	1	1	0	1	0	0	–46 dB
	0	0	0	1	1	0	0	-48 dB
	1	0	0	1	1	0	0	–50 dB
	0	1	0	1	1	0	0	–52 dB
	1	1	0	1	1	0	0	–54 dB
	0	0	1	1	1	0	0	–56 dB
	1	0	1	1	1	0	0	–58 dB
	0	1	1	1	1	0	0	–60 dB
	1	1	1	1	1	0	0	–62 dB
	0	0	0	0	0	1	0	–64 dB
	1	0	0	0	0	1	0	–66 dB
	0	1	0	0	0	1	0	–68 dB
	1	1	0	0	0	1	0	–70 dB
	0	0	1	0	0	1	0	–72 dB
	1	0	1	0	0	1	0	–74 dB
	0	1	1	0	0	1	0	–76 dB
	1	1	1	0	0	1	0	–78 dB
								Mute
	1	1	1	1	1	1	0	

#### Three-band equalizer control

D16	D17	D18	D19	f1 band
D20	D21	D22	D23	f2 band
D24	D25	D26	D27	f3 band
0	1	1	0	+12 dB
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	-2 dB
0	1	0	1	-4 dB
1	1	0	1	6 dB
0	0	1	1	-8 dB
1	0	1	1	-10 dB
0	1	1	1	–12 dB

#### Fader Volume Control

D28	D29	D30	D31	Operation
0	0	0	0	0 dB
1	0	0	0	-1 dB
0	1	0	0	-2 dB
1	1	0	0	-4 dB
0	0	1	0	6 dB
1	0	1	0	8 dB
0	1	1	0	-10 dB
1	1	1	0	-12 dB
0	0	0	1	-14 dB
1	0	0	1	–16 dB
0	1	0	1	–18 dB
1	1	0	1	-20 dB
0	0	1	1	-30 dB
1	0	1	1	-45 dB
0	1	1	1	-60 dB
1	1	1	1	

#### Channel Selection Control

D32	D33	Setting
0	0	Left and right together. This is the mode set up initially
1	0	RCH
0	1	LCH
1	1	Left and right together

#### Fader Rear/Front Control

D34	Setting
0	Rear
1	Front

#### Loudness Control

D35		Setting
0	Off	
1	On	

#### Zero Cross Control

D36	D37	Setting
0	0	Data is written when a zero cross is detected
1	1	The zero cross detection operation is disabled and data is written on the falling edge of the CE signal

#### Zero Cross Signal Detection Block Control

D38	D39	D40	D41	Setting
0	0	0	0	Selector
1	0	0	0	Volume
0	1	0	0	Tone
1	1	0	0	Fader

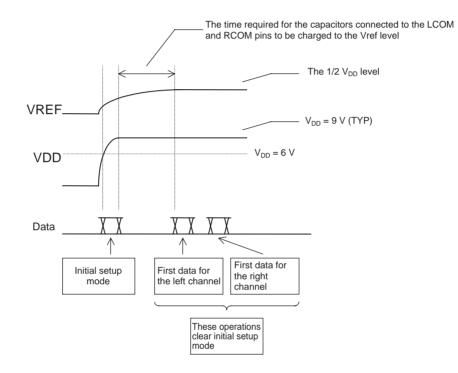
## Test Mode Control

D42	D43	Setting
0	0	These IC test mode control bits must be set to 0

#### **Usage Notes**

Data Transmission after Power Is First Applied

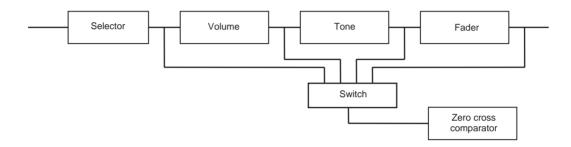
- When power is first applied, the state of the internal analog switches will be undefined. Applications that use this IC must include external circuits to provide muting until control data has been transferred to the IC.
- After power is first applied, applications should send initial setup data to stabilize the bias levels in each of the IC circuit blocks in a short time.
- 1. The time between initial setup mode and the first actual data settings
- Applications should send the initial setup data as soon as V<sub>DD</sub> rises above 6 V.
- After the LCOM and RCOM pins have stabilized at the Vref level, applications should set the initial data.



- 2. Procedure for setting up initial setup mode
- When D32 and D33 are set to 00, the IC's internal initial setup switch is turned on and the IC goes to quick charge mode. At this time the other data (D0 to D31 and D34 to D43) will also be set up for the left and right channels at the same time. This means that applications can set up the states of the various blocks at the same time as specifying initial setup mode.
- 3. Procedure for clearing initial setup mode
- Initial setup mode is cleared by setting D32 and D33 to any value other than 00. In other words, any normal left or right channel specification will turn the internal initial setup switch off and clear quick charge mode.

Zero Cross Switching Circuit Operating Principles

• The LC75384NE-R/NW include functions for switching the place where the zero cross comparator operates and thus allows applications to select the optimal detection location for the block for which the control data is updated. Basically, switching noise will be minimized if the signal immediately following the block for which the control data is updated is input to the zero cross comparator. Thus the detection location must be changed for each data update operation. Another issue is the point that if the signal amplitude is lower than the detection sensitivity (a few mV rms) of the zero cross comparator (for example if the volume is set to a low level), the switching noise can be minimized further by selecting a point before the volume control block, namely the selector block output, as the zero cross timer. For example, if the volume block input is 1 V rms, and the volume is set to -40 dB or lower, the output will be under 10 mV rms. In this case, detecting at the selector output block will result in lower switching noise.



#### **Zero Cross Detection Circuit**

Zero Cross Switching Control Procedure

• The zero cross switching control procedure consists of first setting the zero cross detection mode with the zero cross control bits (D36 and D37 = 0) and then, after specifying the detection block (with bits D38, D39, D40, and D41), sending the control data. Since these control bits are latched first immediately after the data is sent, i.e. on the falling edge of the CE signal, it is possible to both set the IC mode as well as specify zero cross switching operation in a single data transfer, even when updating the volume and other data. The following presents an example of the control operation when updating the volume block data.

D36	D37	D38	D39	D40	D41
0	0	1	0	0	0
$ \subseteq $					
Zero cross mode spe	detection ecification		Volume bl	ock setting	

#### Zero Cross Timer Setting

• When the input signal has a level lower than the detecting sensitivity of the zero cross comparator, or consists only of extremely low frequencies, the zero cross detection circuit will remain in the state in which it cannot detect a zero cross and the data will not be latched during that period. The zero cross timer specifies a time after which the data will be latched forcibly in states where a zero crossing cannot be detected. The time is determined by the lowest frequency for which a zero cross can be detected reliably.

For example, if the timer is set to 25 ms: T = 0.69 CR

If C is taken to be 0.033  $\mu$ F, then R will be:

$$R = \frac{25 \times 10^{-3}}{0.69 \times 0.033 \times 10^{-6}} \approx 1.1 \text{ M}\Omega$$

Notes on Serial Data Transfer

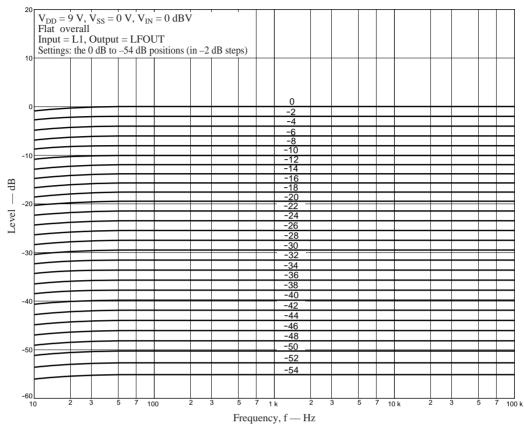
- 1. The CL, DI, and CE pin signal lines must be covered (and thus shielded) by the ground pattern or formed from shielded cable to prevent the high-frequency digital signals on those lines from entering the analog system.
- 2. The LC75384NE-R/NW data formats consist of 8 bits of address and 44 bits of data. When the data is sent in units of 8 bits each (i.e. 48 bits are actually sent), use the data transfer technique shown in figure 1.

LC75384NE-R/NW data receptions in 8-bit units



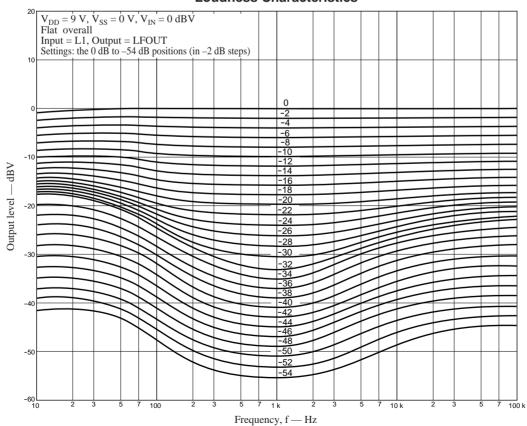
3. During CCB transfers, this IC detects address matches on the rising edge of the CE signal. Therefore, applications must set the CL signal low and then set it high at this time.

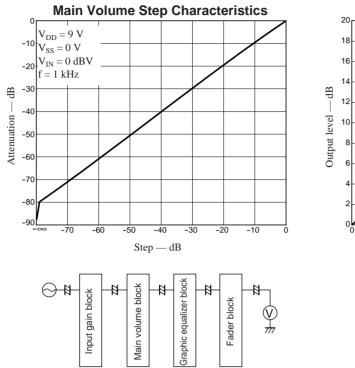
#### LC75384NE-R, 75384NW

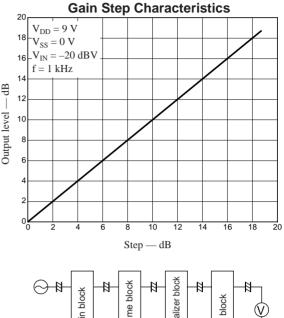


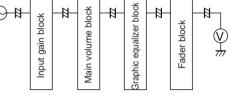
#### **Output Level Characteristics**

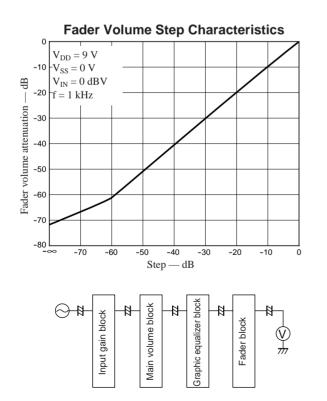
Loudness Characteristics

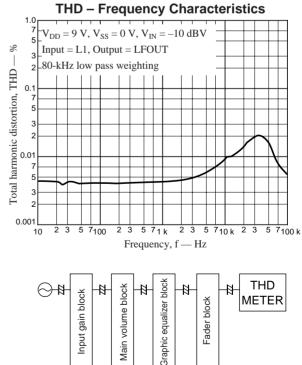


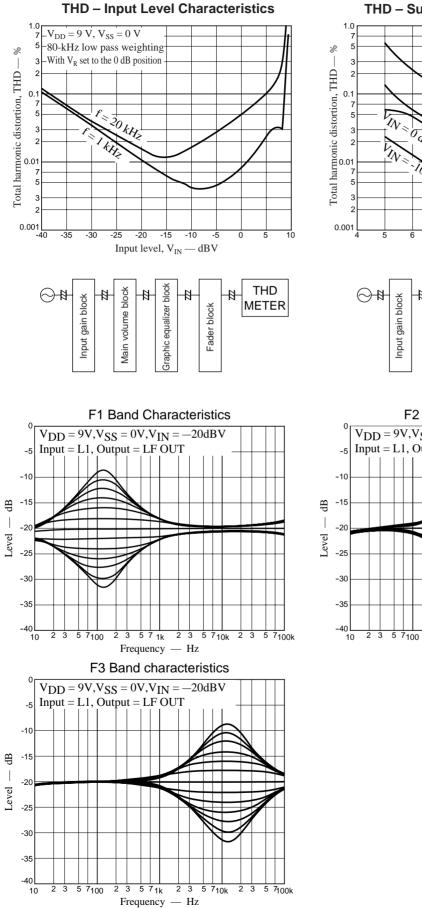






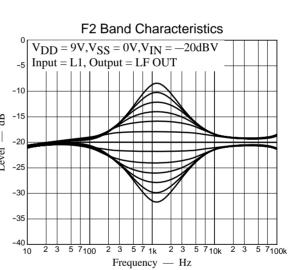








 $V_{SS} = 0 V$ 80-kHz low pass weighting  $V_{IN} = 0 dB_{V, f} = 20 kHz$ The ods v  $V_{IN} =$  $10 \overline{dBV}, f$  $= 20 kH_z$ S I KH2 12 13 10 11 Supply voltage — V Graphic equalizer block THD Main volume block -1 -13 ∄ METER block Fader b



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