Ordering number : ENN6169

CMOS IC

LC75384NE-R, 75384NW

Electronic Volume and Tone Control for Car Stereo Systems

Overview

The LC75384NE-R and LC75384NW are electronic volume and tone control ICs that can implement volume, balance, fader, bass/treble/mid, loudness, input switching, and input gain control functions with a minimum number of external components.

Features

- Volume: 81 positions: from 0 dB to –79 dB in 1-dB steps and –∞.
  A balance function can be implemented by controlling the left and right volume settings independently.
- Fader: Either the rear or front outputs can be attenuated over 16 positions. (16 positions: From 0 dB to –2 dB in 1-dB steps, from –2 dB to –20 dB in 2-dB steps, from –20 to –30 dB in one 10-dB step, –45 dB, –60 dB, and –∞.)
- Bass/treble/mid: Control over ±12 dB in 2-dB steps in each band.
- Input gain: The input signal can be amplified by from 0 dB to +18.75 dB in 1.25-dB steps.
- Input switching: The left and right channels can each be selected from one of 5 inputs. (Four are single-ended inputs and one is a differential input.)
- Loudness: Taps are output from a 2-dB step volume control ladder resistor starting at the –32-dB position. A loudness function can be implemented by attaching external capacitors and resistors.
- On-chip buffer amplifiers minimize the number of required external components.
- Minimal switching noise when no input signals are present due to fabrication in a silicon gate CMOS process that minimizes the noise generated by internal switches.
- Use of zero-cross switching circuits for internal switches minimizes switching noise when signals are present.
- Built-in $V_{DD}/2$ reference voltage generator circuit
- All controls can be set from serial input data.

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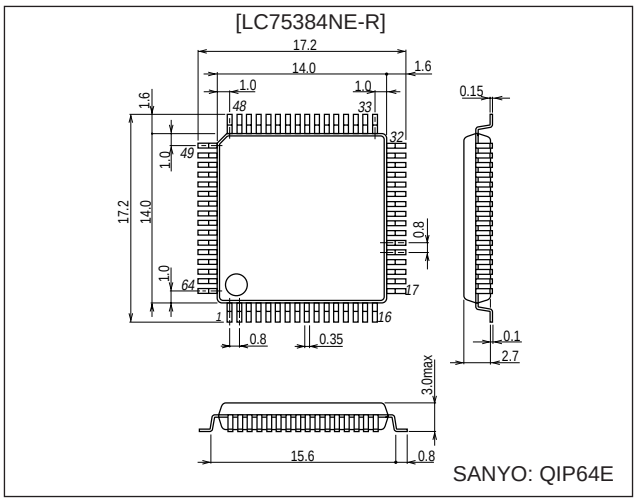
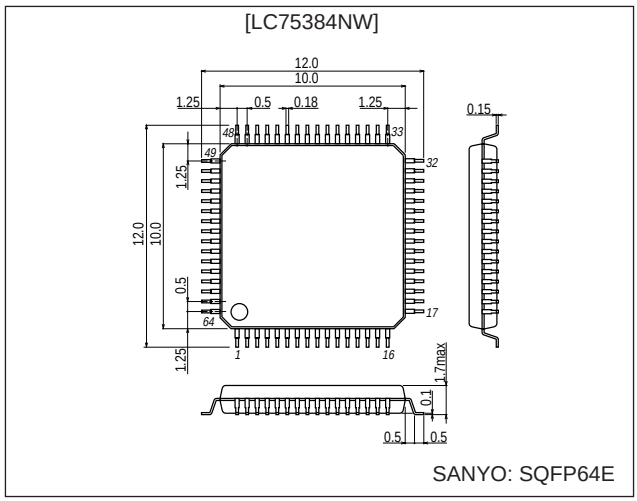
Package Dimensions

unit: mm

3159-QIP64E



3190-SQFP64



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions		Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}		11	V
Maximum input voltage	V_{IN} max	All input pins		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C, when mounted on a printed circuit board	LC75384NE-R	500	mW
			LC75384NW	420	
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–50 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	6.0		10.5	V
Input high-level voltage	V_{IH}	CL, DI, CE, $\overline{\text{MUTE}}$	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE, $\overline{\text{MUTE}}$	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}		V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1			µs
Setup time	t_{setup}	CL, DI, CE	1			µs
Hold time	thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

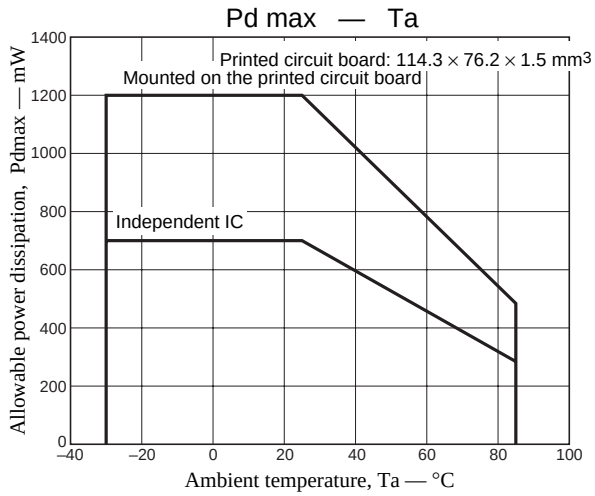
Electrical Characteristics at Ta = 25°C, V_{DD} = 9 V, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				min	typ	max	
[Input Block]							
Input resistance	Rin	L1 to L4, R1 to R4		30	50	70	kΩ
Minimum input gain	Ginmin	L1 to L4, R1 to R4		–1	0	+1	dB
Maximum input gain	Ginmax			+16.5	+18.75	+21	dB
Inter-step setting error	ATerr					±0.6	dB
Left/right balance	BAL					±0.5	dB
[Volume Block]							
Input resistance	Rvr	LVRIN, RVRIN, loudness off		113	226	339	kΩ
Inter-step setting error	ATerr					±0.5	dB
Left/right balance	BAL					±0.5	dB
[Tone Control Block]							
Inter-step setting error	ATerr					±1.0	dB
Bass control range	Gbass		max. boost/cut	±9	±12	±15	dB
Mid control range	Gmid		max. boost/cut	±9	±12	±15	dB
Treble control range	Gtre		max. boost/cut	±9	±12	±15	dB
Left/right balance	BAL					±0.5	dB
[Fader Block]							
Input resistance	Rfed	LFIN, RFIN		25	50	100	kΩ
Inter-step setting error	ATerr		0 dB to –2 dB			±0.5	dB
			–2 dB to –20 dB			±1	dB
			–20 dB to –30 dB			±2	dB
			–30 dB to –60 dB			±3	dB
Left/right balance	BAL					±0.5	dB

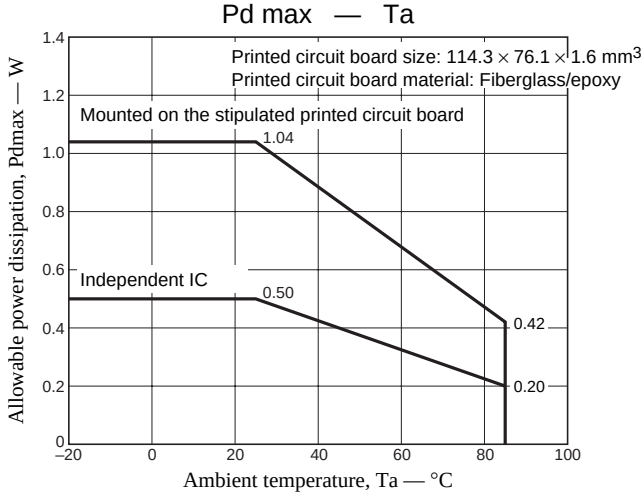
Overall Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD 1	V_{IN} = –10 dBV, f = 1 kHz		0.004		%
	THD 2	V_{IN} = –10 dBV, f = 10 kHz		0.006		%
Inter-input crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
Left/right channel crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
Maximum attenuation	V_{O} min 1	V_{IN} = 1 Vrms, f = 1 kHz	80	88		dB
	V_{O} min 2	V_{IN} = 1 Vrms, f = 1 kHz, INMUTE, with the fader set to –∞	90	95		dB
Output noise voltage	V_{N} 1	All controls flat, with the IHF-A filter		5	10	μV
	V_{N} 2	All controls flat, with a 20 Hz to 20 kHz bandpass filter		7	15	μV
Current drain	I_{DD}			33	40	mA
Input high-level current	I_{IH}	CL, DI, CE, V_{IN} = 9 V			10	μA
Input low-level current	I_{IL}	CL, DI, CE, V_{IN} = 0 V	–10			μA
Maximum input voltage	V_{CL}	THD = 1 %, R_L = 10 kΩ, all controls flat, f_{IN} = 1 kHz	2.5	2.9		Vrms
Common-mode rejection ratio	CMRR	V_{IN} = 0 dBV, f = 1 kHz	45			dB

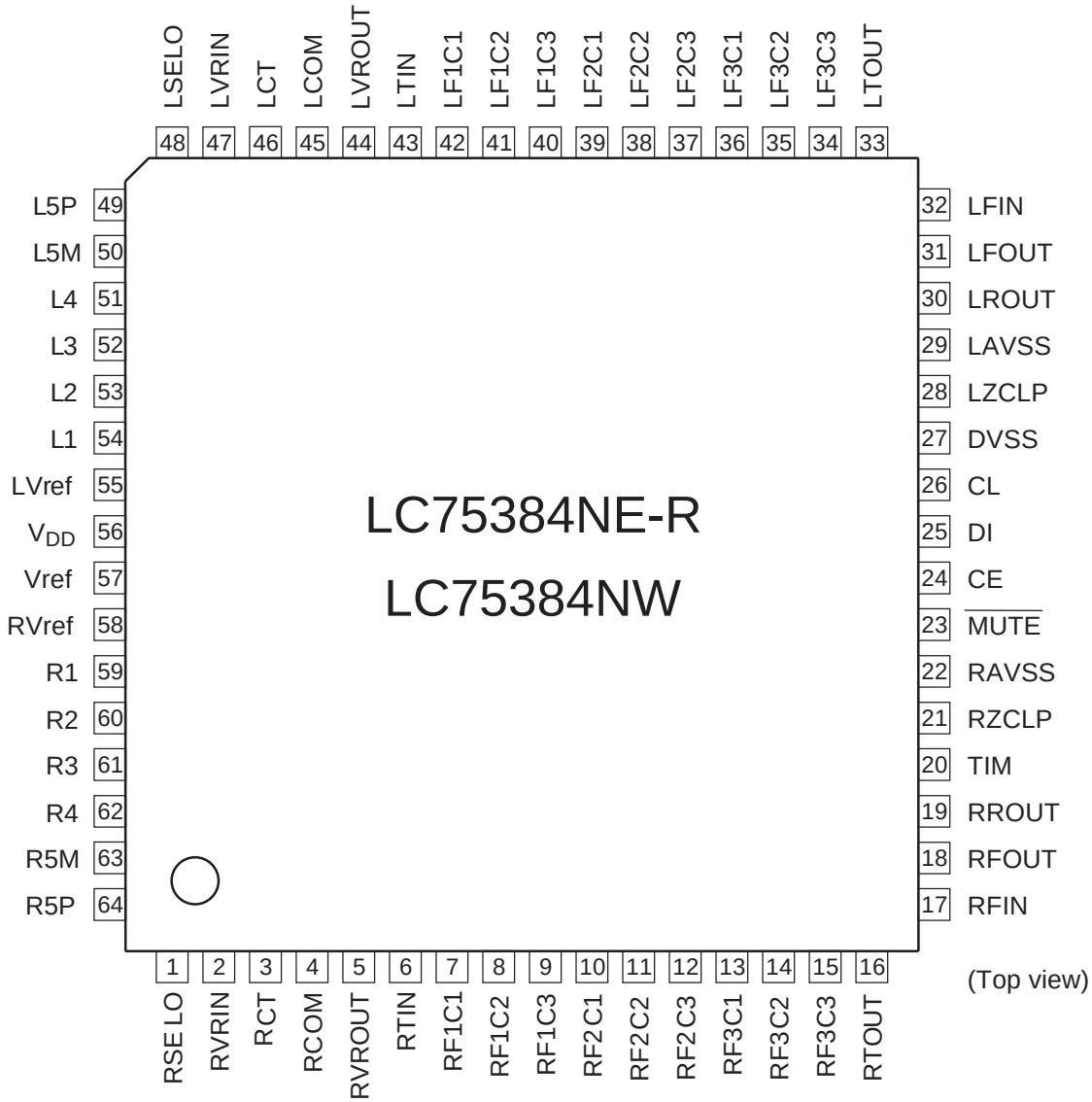
[LC75384NE-R]



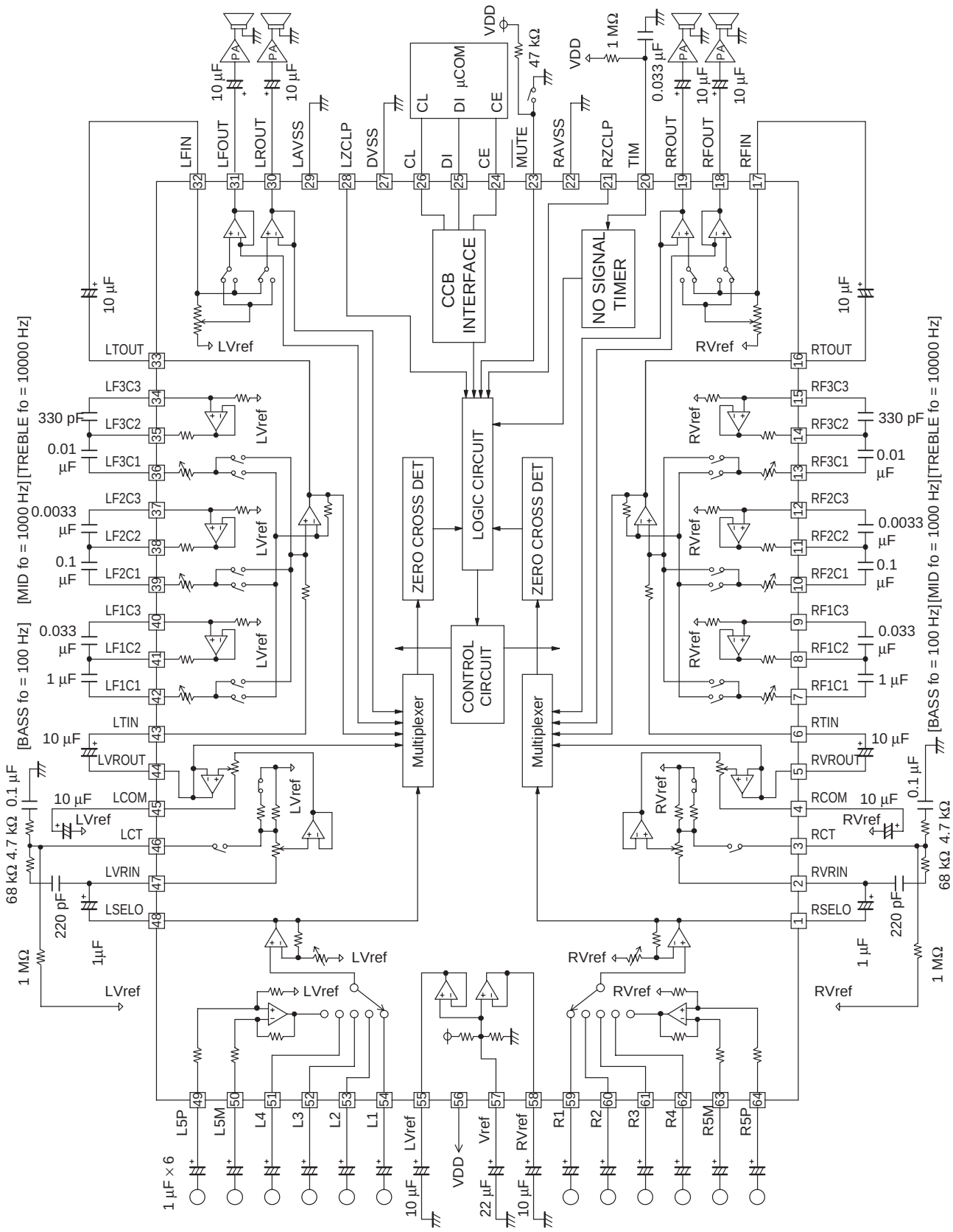
[LC75384NW]



Pin Assignment

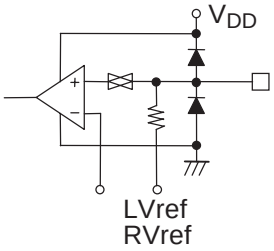
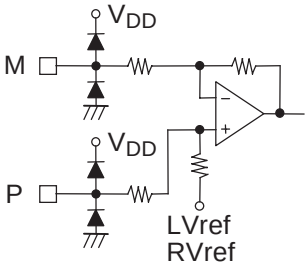
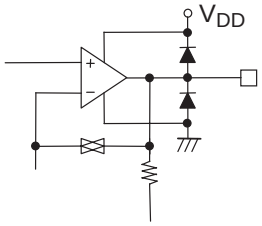
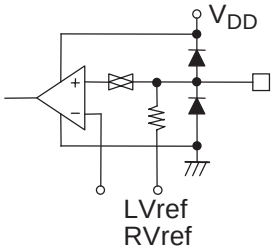
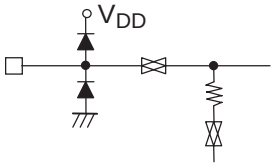
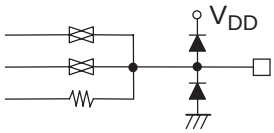
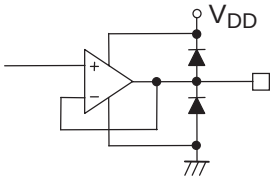


Equivalent Circuit and Sample Application Circuit Diagram



• In the LC75384NW version, LZCLP (pin 28) and RZCLP (pin 21) are unused, and must be left open.

Pin Functions

Pin No.	Pin	Function	Notes
54 53 52 51 59 60 61 62	L1 L2 L3 L4 R1 R2 R3 R4	• Single end inputs	
50 49 63 64	L5M L5P R5M R5P	• Differential inputs	
48 1	LSEL0 RSEL0	• Input selector outputs	
47 2	LVRIN RVRIN	• Inputs for the 2-dB step volume control • These inputs must be driven from low-impedance circuits.	
46 3	LCT RCT	• Loudness function pins. Connect the high-band compensation RC circuits between the LCT (RCT) and the LVRIN (RVRIN) pins and connect the low-band compensation RC circuits between the LCT (RCT) and LVREF (RVREF).	
45 4	LCOM RCOM	• 2-dB step volume control outputs • To reduce switching noise, each of these pins should be connected to LVREF (RVREF) through a capacitor.	
44 5	LVROUT RVROUT	• Output from the 1-dB step volume control	

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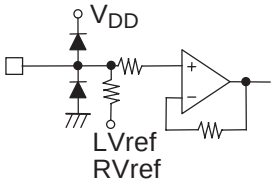
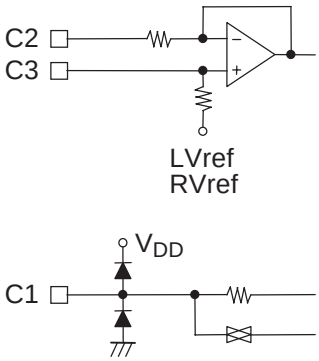
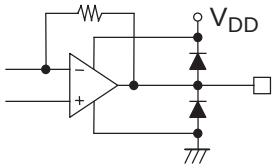
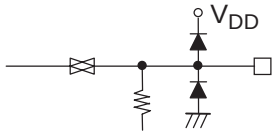
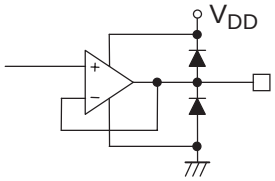
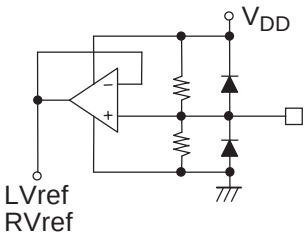
Pin No.	Pin	Function	Equivalent circuit
43 6	LTIN RTIN	• Equalizer input	
42 41 40 7 8 9	LF1C1 LF1C2 LF1C3 RF1C1 RF1C2 RF1C3	• Connections for the capacitors for the equalizer's F1 band filter. The low band compensation capacitors must be connected between the following pins: LF1C1 (RF1C1) and LF1C2 (RF1C2) LF1C2 (RF1C2) and LF1C3 (RF1C3)	
39 38 37 10 11 12	LF2C1 LF2C2 LF2C3 RF2C1 RF2C2 RF2C3	• Connections for the capacitors for the equalizer's F2 band filter. The low band compensation capacitors must be connected between the following pins: LF2C1 (RF2C1) and LF2C2 (RF2C2) LF2C2 (RF2C2) and LF2C3 (RF2C3)	
36 35 34 13 14 15	LF3C1 LF3C2 LF3C3 RF3C1 RF3C2 RF3C3	• Connections for the capacitors for the equalizer's F3 band filter. The low band compensation capacitors must be connected between the following pins: LF3C1 (RF3C1) and LF3C2 (RF3C2) LF3C2 (RF3C2) and LF3C3 (RF3C3)	
33 16	LTOUT RTOUT	• Equalizer output	
32 17	LFIN RFIN	• Fader block inputs • These inputs must be driven from low-impedance circuits.	
31 30 18 19	LFOUT LROUT RFOUT RROUT	• Fader block outputs. The front and rear outputs can be attenuated independently. The attenuation is the same in the left and right channels.	
57	Vref	• V_{DD}/2 voltage generator block. A capacitor with a value of about 10 µF must be inserted between Vref and AV_{SS} (V_{SS}) to reduce power supply ripple.	
55 58	LVref RVref	• Internal analog system ground • These pins must be handled as shown in the sample application circuit.	

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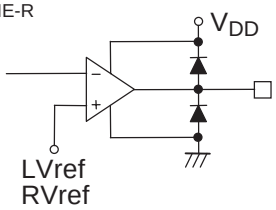
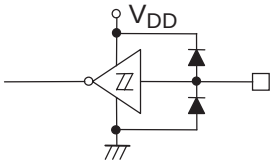
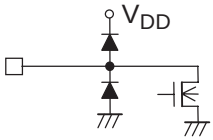
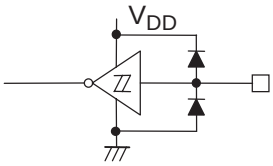
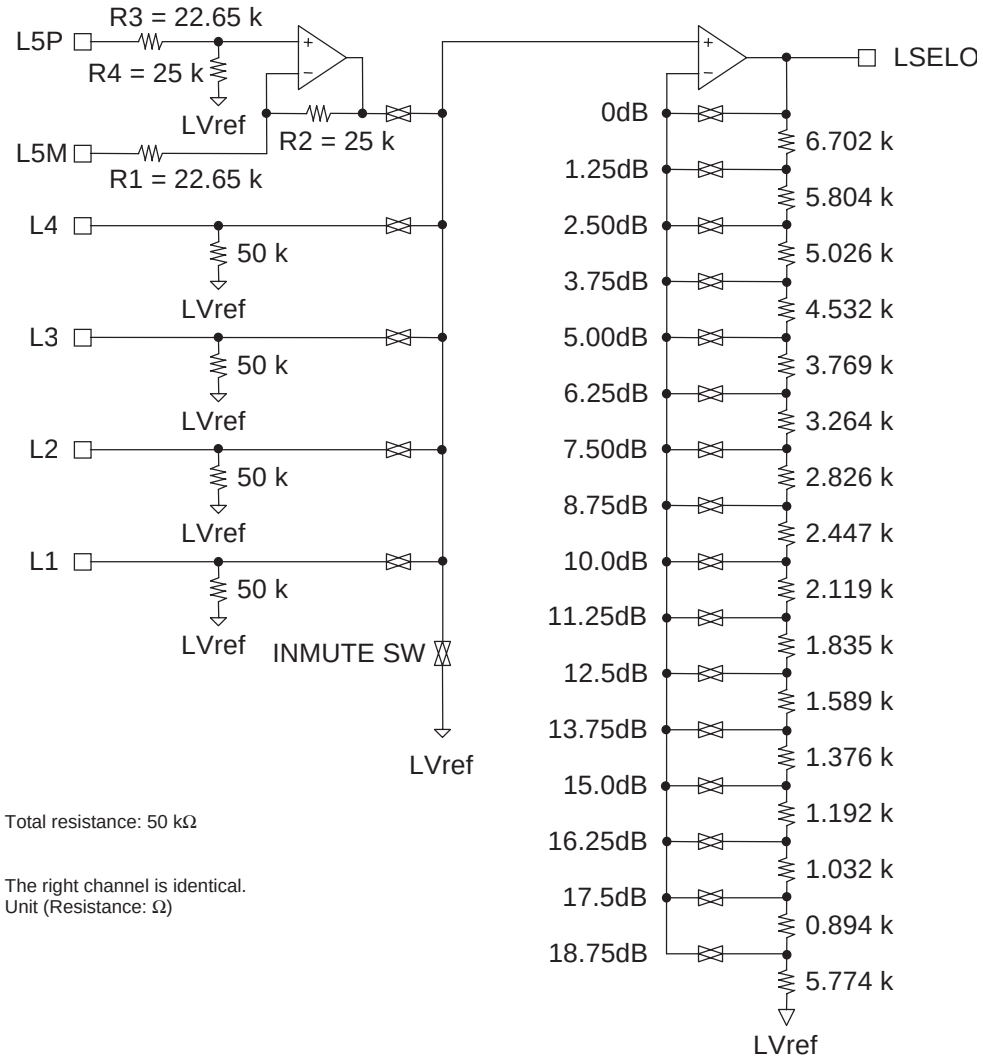
Pin No.	Pin	Function	Equivalent circuit
56	V_{DD}	• Power supply	
27	DV_{SS}	• Logic system ground	
29 22	LAV_{SS} RAV_{SS}	• Analog system ground	
28 21	LZCLP RZCLP	• Band limiting for the zero cross detection circuit • These pins are normally left open. • These pins are unused in the LC75384NW version and must be left open.	LC75384NE-R 
23	$\overline{\text{MUTE}}$	• External muting control • When this pin is set to the V_{SS} level, the fader volume block is forcibly set to –∞.	
20	TIM	• Used for the zero cross circuit no-signal timer function. If a zero cross signal does not occur between the point when data is loaded and the point when the timer times out, the data will be stored forcibly when the timer times out.	
26 25	CL DI	• Serial data and clock inputs used for device control	
24	CE	• Chip enable input. Data is written to the internal latch when this pin goes from high to low. The analog switches then operate. Data transfers are enabled when this pin is high.	

Internal Equivalent Circuits

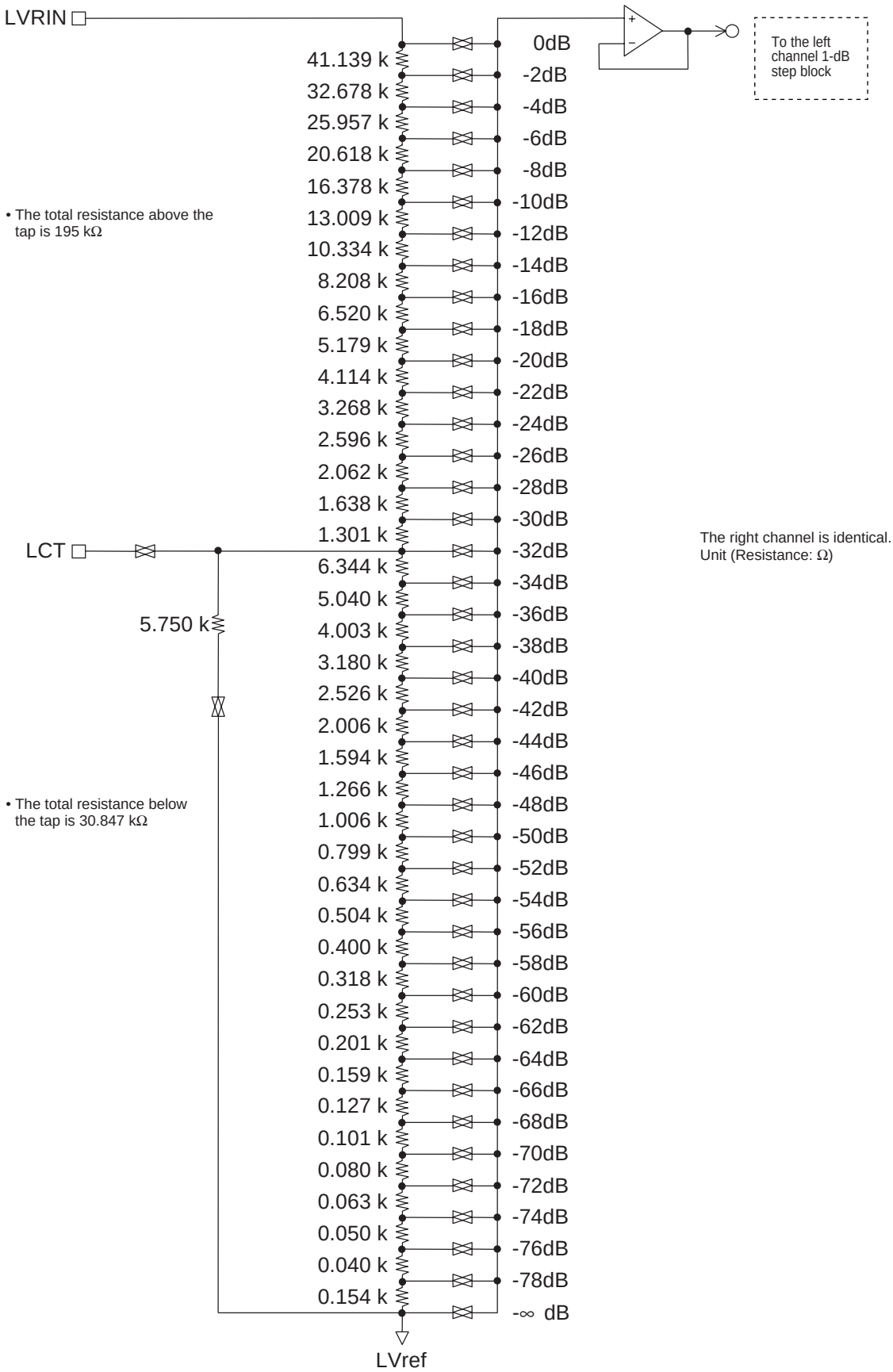
Selector Block Equivalent Circuit



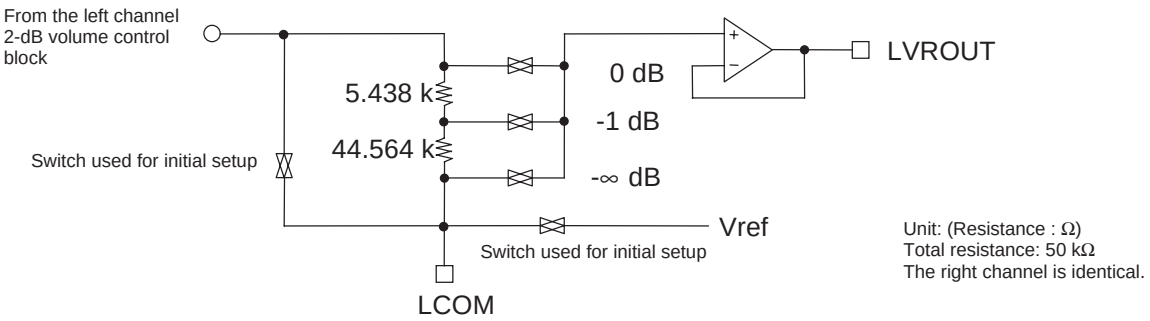
Total resistance: 50 kΩ

The right channel is identical.
Unit (Resistance: Ω)

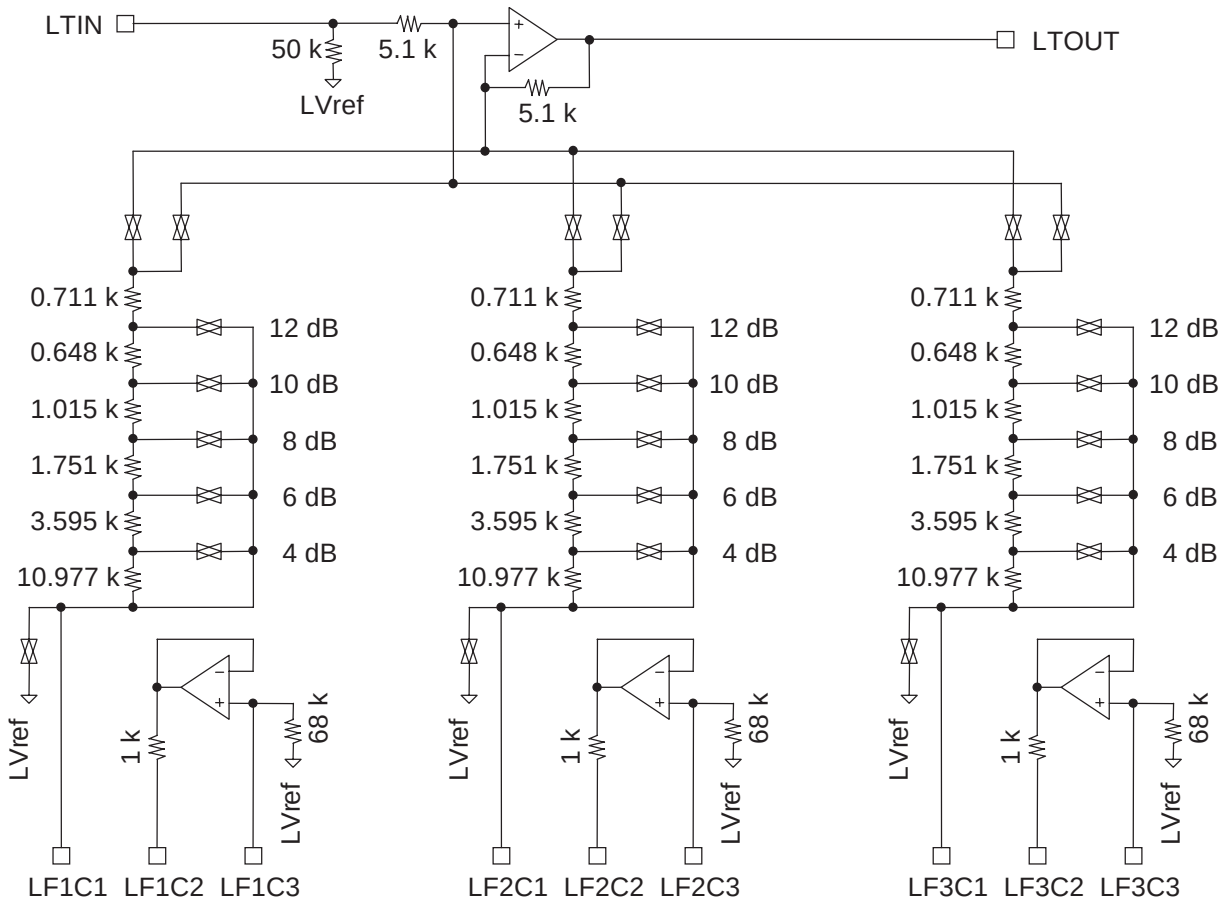
2-dB Step Volume Control Block Equivalent Circuit



1-dB Step Volume Control Block Equivalent Circuit



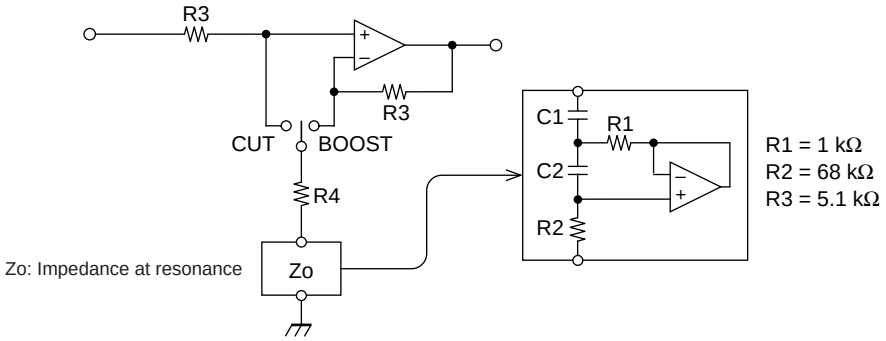
Three-Band Graphic Equalizer Block Equivalent Circuit Diagram



Unit: (Resistance : Ω)

The external capacitors C1 and C2 used with the LC75384W form the structural element of the simulated inductor implemented by the IC. This section present the equivalent circuit and the method for calculating the constants required to obtain the desired center frequency.

(A) Simulated inductor equivalent circuit



(B) Calculation

Specifications: 1. Center frequency: F_0 = 100 Hz

2. Q at maximum boost: Q_{+12dB} = 0.9

1. Determine the sharpness, Q_0, of the simulated inductor itself.

$$Q0 = \frac{(R1 + R4)}{R1} \times Q_{+12dB} \approx 1.5399$$

2. Determine C1.

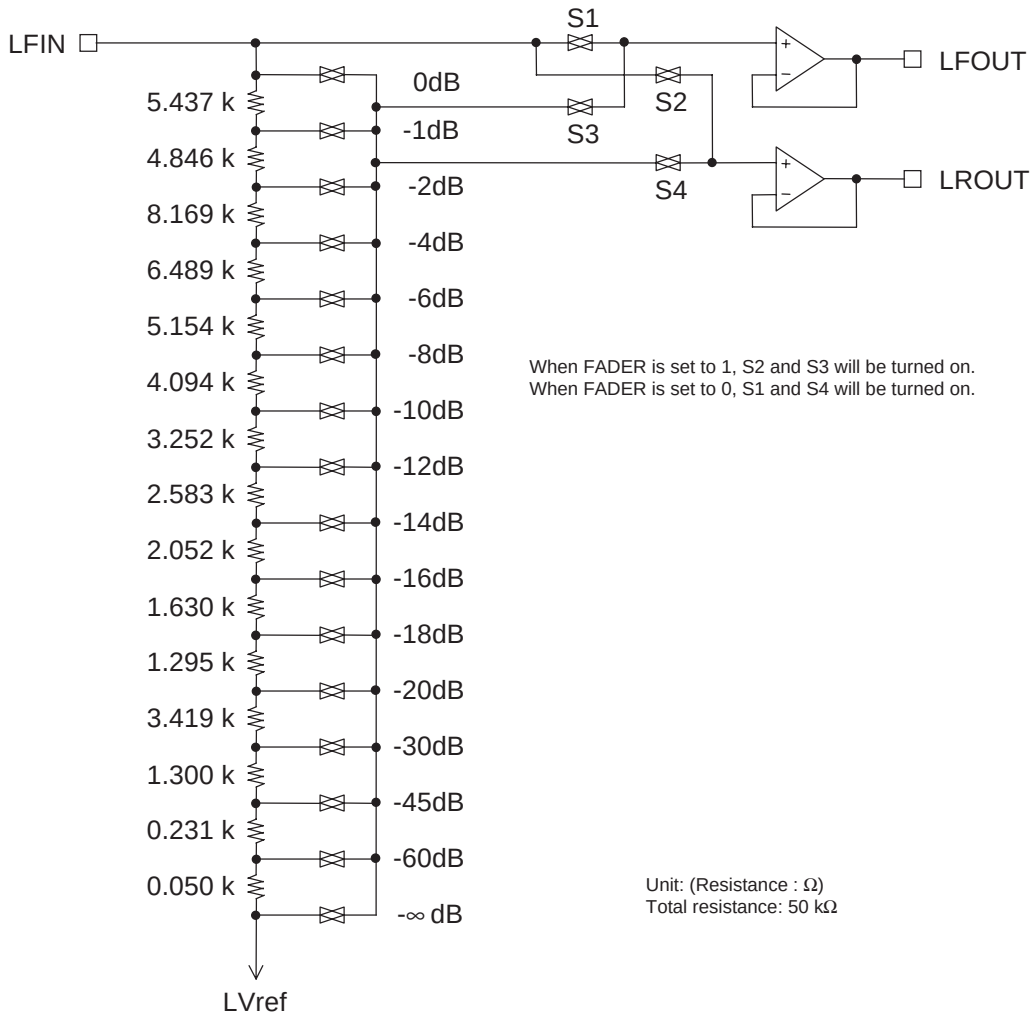
$$C1 = 1/2\pi F_0 R1 Q_0 \neq 1\ (\mu F)$$

3. Determine C2.

$$C2 = Q_0/2\pi F_0 R2 \neq 0.036\ (\mu F)$$

Note: * See the equivalent circuit diagram for the tone control block on page 11 for details on the internal resistor.

Fader Volume Control Block Equivalent Circuit



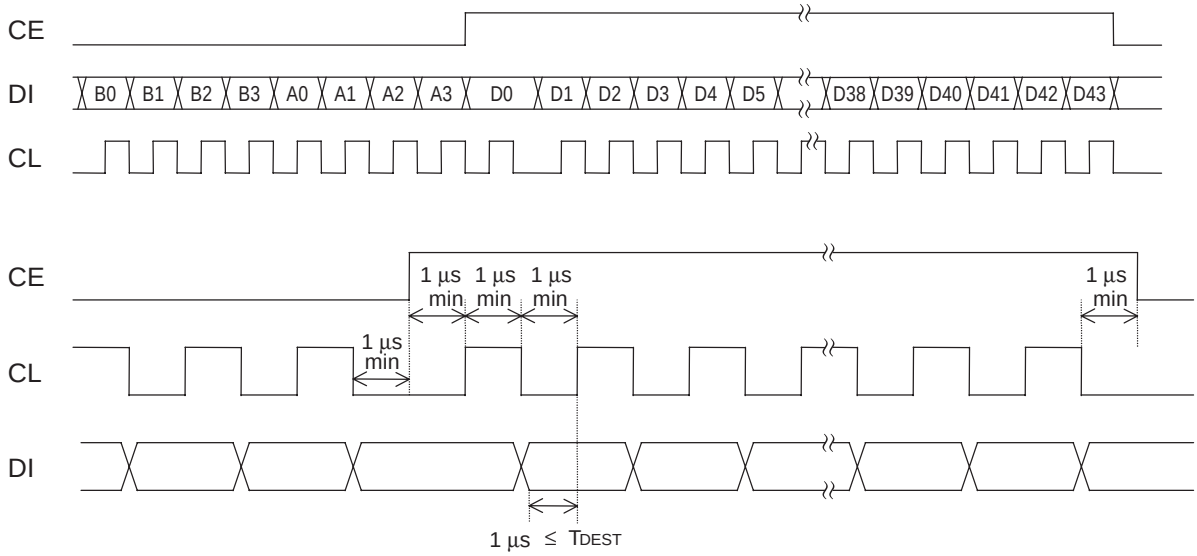
When FADER is set to 1, S2 and S3 will be turned on.
When FADER is set to 0, S1 and S4 will be turned on.

Unit: (Resistance : Ω)
Total resistance: 50 kΩ

If data that sets the main volume control 1-dB step circuit to –∞ is sent to the device, switches S1 and S2 will be opened (off) and switches S3 and S4 will be closed (on).

Control System Timing and Data Format

The LC75384NE-R/NW are controlled by applying the stipulated data to the CL, DI, and CE pins. The data consists of a total of 52 bits, of which 8 bits are the device address and 44 bits are the actual control data.



- Address code (B0 to A3)
  The LC75384NE-R/NW have an 8-bit address codes, and can be used along with other ICs that support the Sanyo CCB serial bus.

  Address code

(LSB)	B0	B1	B2	B3	A0	A1	A2	A3	(81HEX)
	1	0	0	0	0	0	0	1	

- Control code allocation

  Input switching control

D0	D1	D2	Setting	
0	0	0	L1 (R1)	
1	0	0	L2 (R2)	
0	1	0	L3 (R3)	
1	1	0	L4 (R4)	
0	0	1	L5 (R5)	
0	1	1		IC test values. These values must not be used during normal operation.
1	1	1		

D3	IC test bit. This bit must be set to 0 during normal operation.

Input gain control

D4	D5	D6	D7	Operation
0	0	0	0	0 dB
1	0	0	0	+1.25 dB
0	1	0	0	+2.50 dB
1	1	0	0	+3.75 dB
0	0	1	0	+5.00 dB
1	0	1	0	+6.25 dB
0	1	1	0	+7.50 dB
1	1	1	0	+8.75 dB
0	0	0	1	+10.0 dB
1	0	0	1	+11.25 dB
0	1	0	1	+12.5 dB
1	1	0	1	+13.75 dB
0	0	1	1	+15.0 dB
1	0	1	1	+16.25 dB
0	1	1	1	+17.5 dB
1	1	1	1	+18.75 dB

Volume Control

D8	D9	D10	D11	D12	D13	D14	D15	Operation
								1-dB step
0								0 dB
1								–1 dB
								2-dB step
	0	0	0	0	0	0	0	0 dB
	1	0	0	0	0	0	0	–2 dB
	0	1	0	0	0	0	0	–4 dB
	1	1	0	0	0	0	0	–6 dB
	0	0	1	0	0	0	0	–8 dB
	1	0	1	0	0	0	0	–10 dB
	0	1	1	0	0	0	0	–12 dB
	1	1	1	0	0	0	0	–14 dB
	0	0	0	1	0	0	0	–16 dB
	1	0	0	1	0	0	0	–18 dB
	0	1	0	1	0	0	0	–20 dB
	1	1	0	1	0	0	0	–22 dB
	0	0	1	1	0	0	0	–24 dB
	1	0	1	1	0	0	0	–26 dB
	0	1	1	1	0	0	0	–28 dB
	1	1	1	1	0	0	0	–30 dB
	0	0	0	0	1	0	0	–32 dB
	1	0	0	0	1	0	0	–34 dB
	0	1	0	0	1	0	0	–36 dB
	1	1	0	0	1	0	0	–38 dB
	0	0	1	0	1	0	0	–40 dB
	1	0	1	0	1	0	0	–42 dB
	0	1	1	0	1	0	0	–44 dB
	1	1	1	0	1	0	0	–46 dB
	0	0	0	1	1	0	0	–48 dB
	1	0	0	1	1	0	0	–50 dB
	0	1	0	1	1	0	0	–52 dB
	1	1	0	1	1	0	0	–54 dB
	0	0	1	1	1	0	0	–56 dB
	1	0	1	1	1	0	0	–58 dB
	0	1	1	1	1	0	0	–60 dB
	1	1	1	1	1	0	0	–62 dB
	0	0	0	0	0	1	0	–64 dB
	1	0	0	0	0	1	0	–66 dB
	0	1	0	0	0	1	0	–68 dB
	1	1	0	0	0	1	0	–70 dB
	0	0	1	0	0	1	0	–72 dB
	1	0	1	0	0	1	0	–74 dB
	0	1	1	0	0	1	0	–76 dB
	1	1	1	0	0	1	0	–78 dB
								Mute
	1	1	1	1	1	1	0	–∞

Three-band equalizer control

D16	D17	D18	D19	f1 band
D20	D21	D22	D23	f2 band
D24	D25	D26	D27	f3 band
0	1	1	0	+12 dB
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	–2 dB
0	1	0	1	–4 dB
1	1	0	1	–6 dB
0	0	1	1	–8 dB
1	0	1	1	–10 dB
0	1	1	1	–12 dB

Fader Volume Control

D28	D29	D30	D31	Operation
0	0	0	0	0 dB
1	0	0	0	–1 dB
0	1	0	0	–2 dB
1	1	0	0	–4 dB
0	0	1	0	–6 dB
1	0	1	0	–8 dB
0	1	1	0	–10 dB
1	1	1	0	–12 dB
0	0	0	1	–14 dB
1	0	0	1	–16 dB
0	1	0	1	–18 dB
1	1	0	1	–20 dB
0	0	1	1	–30 dB
1	0	1	1	–45 dB
0	1	1	1	–60 dB
1	1	1	1	–∞

Channel Selection Control

D32	D33	Setting
0	0	Left and right together. This is the mode set up initially
1	0	RCH
0	1	LCH
1	1	Left and right together

Fader Rear/Front Control

D34	Setting
0	Rear
1	Front

Loudness Control

D35	Setting
0	Off
1	On

Zero Cross Control

D36	D37	Setting
0	0	Data is written when a zero cross is detected
1	1	The zero cross detection operation is disabled and data is written on the falling edge of the CE signal

Zero Cross Signal Detection Block Control

D38	D39	D40	D41	Setting
0	0	0	0	Selector
1	0	0	0	Volume
0	1	0	0	Tone
1	1	0	0	Fader

Test Mode Control

D42	D43	Setting
0	0	These IC test mode control bits must be set to 0

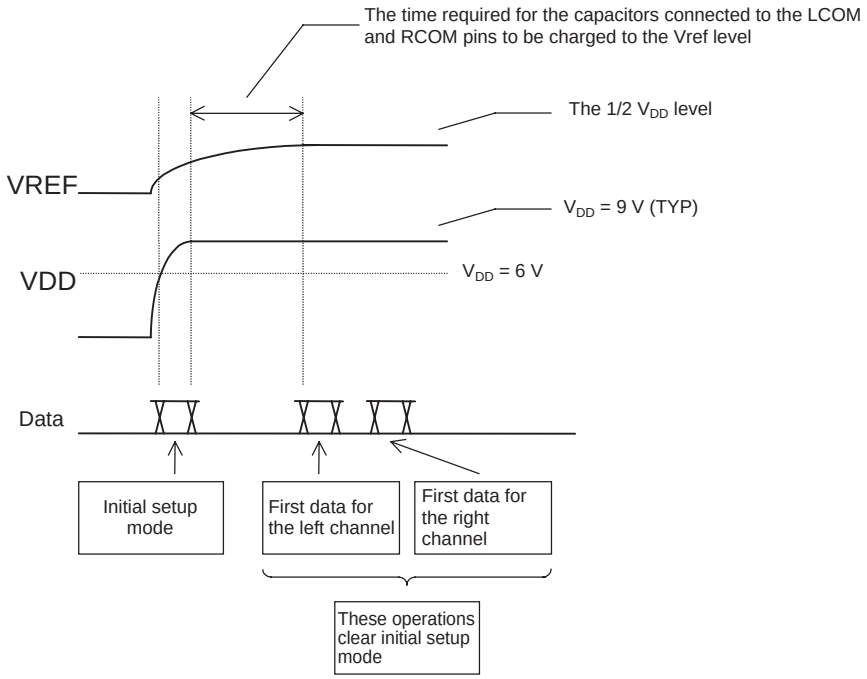
Usage Notes

Data Transmission after Power Is First Applied

- When power is first applied, the state of the internal analog switches will be undefined. Applications that use this IC must include external circuits to provide muting until control data has been transferred to the IC.
- After power is first applied, applications should send initial setup data to stabilize the bias levels in each of the IC circuit blocks in a short time.

1. The time between initial setup mode and the first actual data settings

- Applications should send the initial setup data as soon as V_{DD} rises above 6 V.
- After the LCOM and RCOM pins have stabilized at the Vref level, applications should set the initial data.



2. Procedure for setting up initial setup mode

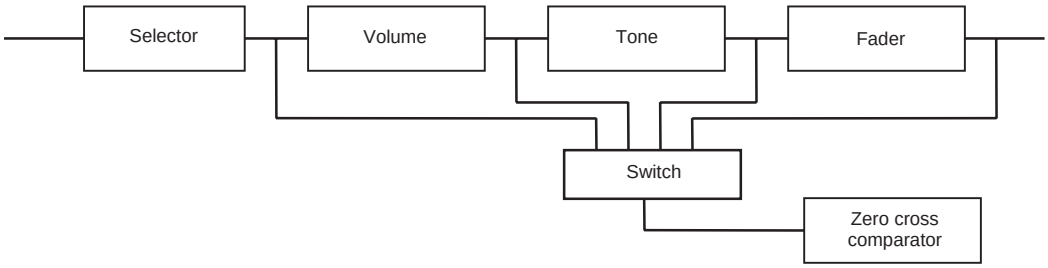
- When D32 and D33 are set to 00, the IC's internal initial setup switch is turned on and the IC goes to quick charge mode. At this time the other data (D0 to D31 and D34 to D43) will also be set up for the left and right channels at the same time. This means that applications can set up the states of the various blocks at the same time as specifying initial setup mode.

3. Procedure for clearing initial setup mode

- Initial setup mode is cleared by setting D32 and D33 to any value other than 00. In other words, any normal left or right channel specification will turn the internal initial setup switch off and clear quick charge mode.

Zero Cross Switching Circuit Operating Principles

- The LC75384NE-R/NW include functions for switching the place where the zero cross comparator operates and thus allows applications to select the optimal detection location for the block for which the control data is updated. Basically, switching noise will be minimized if the signal immediately following the block for which the control data is updated is input to the zero cross comparator. Thus the detection location must be changed for each data update operation. Another issue is the point that if the signal amplitude is lower than the detection sensitivity (a few mV rms) of the zero cross comparator (for example if the volume is set to a low level), the switching noise can be minimized further by selecting a point before the volume control block, namely the selector block output, as the zero cross detection point than by simply waiting for the data write to occur due to the overflow of the zero cross timer. For example, if the volume block input is 1 V rms, and the volume is set to –40 dB or lower, the output will be under 10 mV rms. In this case, detecting at the selector output block will result in lower switching noise.



Zero Cross Detection Circuit

Zero Cross Switching Control Procedure

- The zero cross switching control procedure consists of first setting the zero cross detection mode with the zero cross control bits (D36 and D37 = 0) and then, after specifying the detection block (with bits D38, D39, D40, and D41), sending the control data. Since these control bits are latched first immediately after the data is sent, i.e. on the falling edge of the CE signal, it is possible to both set the IC mode as well as specify zero cross switching operation in a single data transfer, even when updating the volume and other data. The following presents an example of the control operation when updating the volume block data.

D36	D37	D38	D39	D40	D41
0	0	1	0	0	0

Zero cross detection mode specification

Volume block setting

Zero Cross Timer Setting

- When the input signal has a level lower than the detecting sensitivity of the zero cross comparator, or consists only of extremely low frequencies, the zero cross detection circuit will remain in the state in which it cannot detect a zero cross and the data will not be latched during that period. The zero cross timer specifies a time after which the data will be latched forcibly in states where a zero crossing cannot be detected. The time is determined by the lowest frequency for which a zero cross can be detected reliably.

For example, if the timer is set to 25 ms:

$$T = 0.69\ CR$$

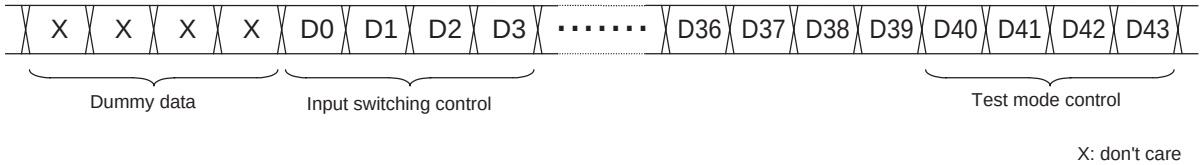
If C is taken to be 0.033 µF, then R will be:

$$R = \frac{25 \times 10^{-3}}{0.69 \times 0.033 \times 10^{-6}} \approx 1.1\ M\Omega$$

Notes on Serial Data Transfer

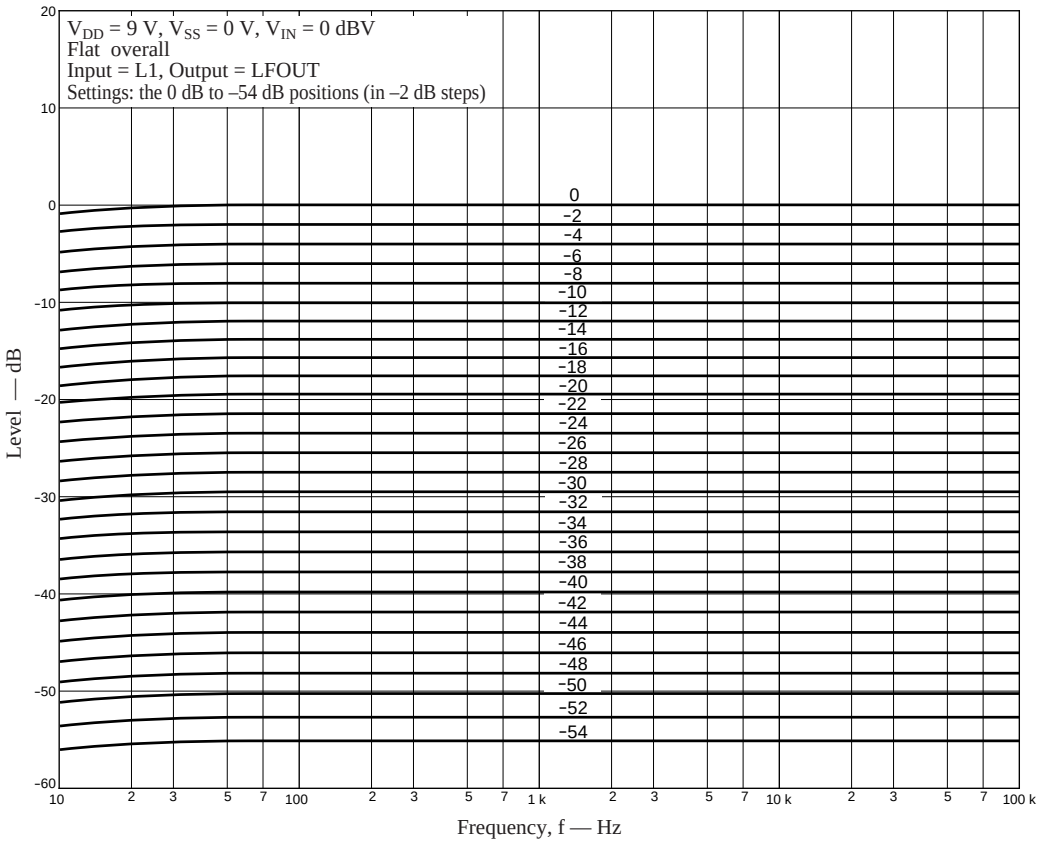
1. The CL, DI, and CE pin signal lines must be covered (and thus shielded) by the ground pattern or formed from shielded cable to prevent the high-frequency digital signals on those lines from entering the analog system.
2. The LC75384NE-R/NW data formats consist of 8 bits of address and 44 bits of data. When the data is sent in units of 8 bits each (i.e. 48 bits are actually sent), use the data transfer technique shown in figure 1.

LC75384NE-R/NW data receptions in 8-bit units

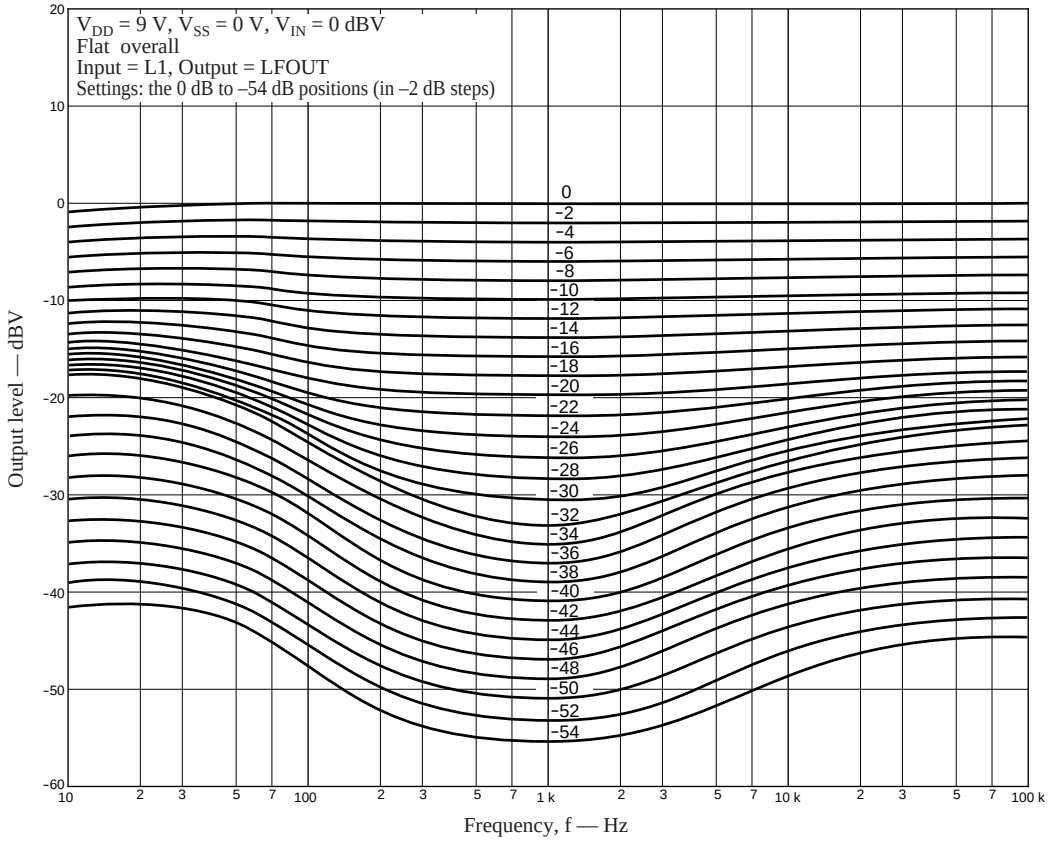


3. During CCB transfers, this IC detects address matches on the rising edge of the CE signal. Therefore, applications must set the CL signal low and then set it high at this time.

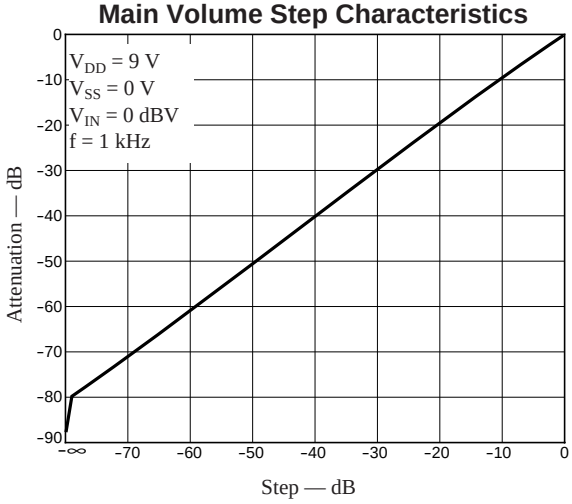
Output Level Characteristics

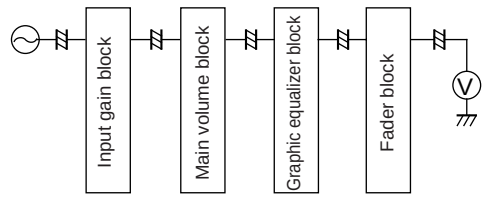


Loudness Characteristics

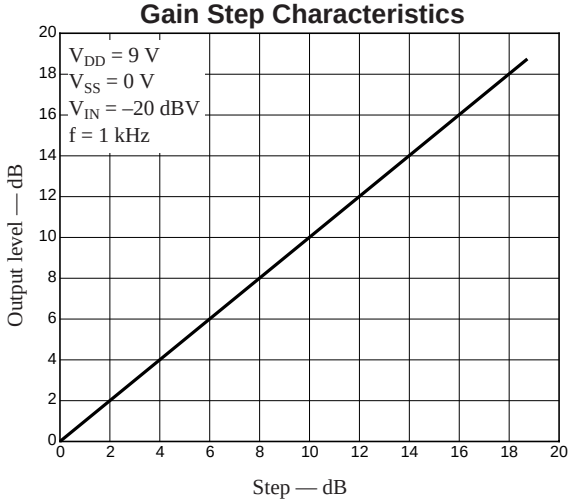


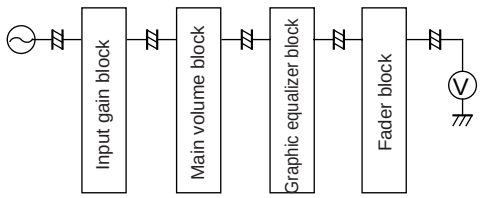
Main Volume Step Characteristics



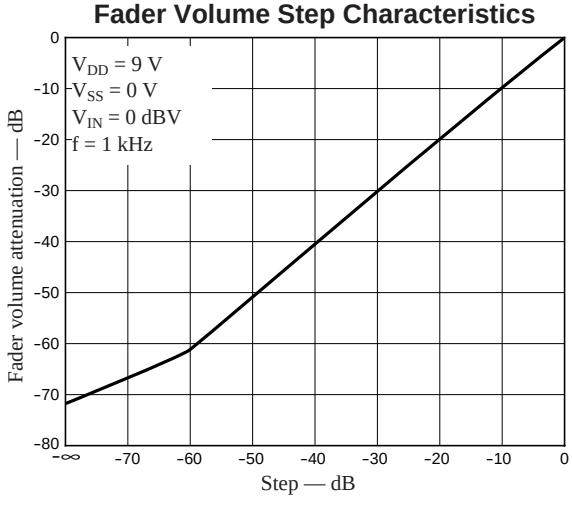


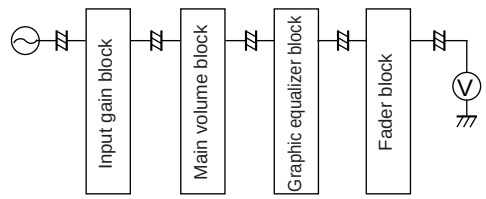
Gain Step Characteristics



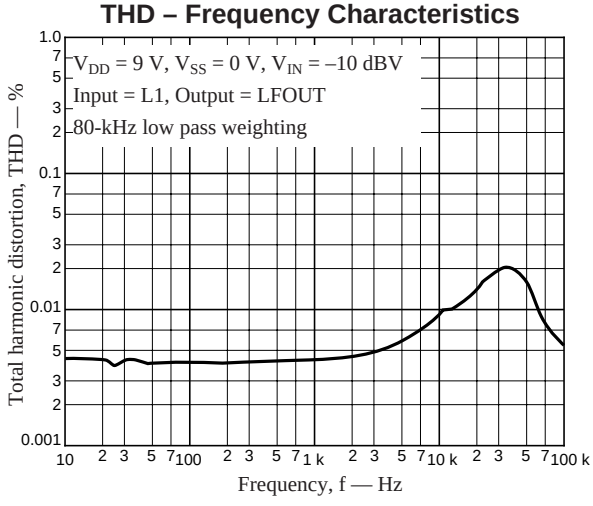


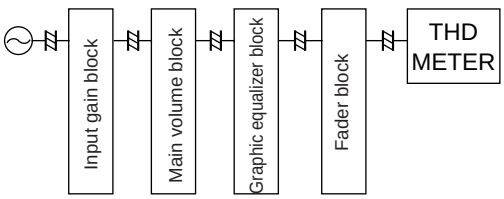
Fader Volume Step Characteristics



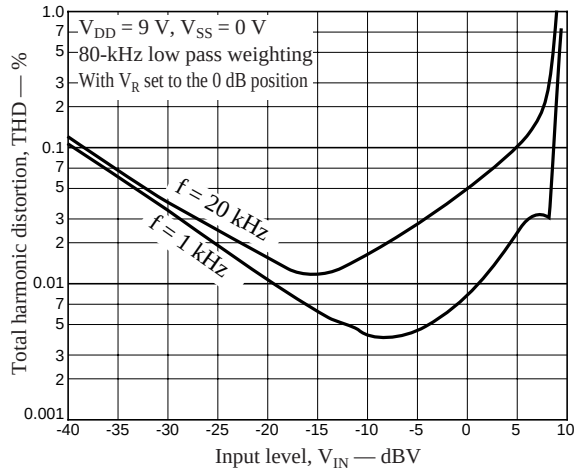


THD – Frequency Characteristics

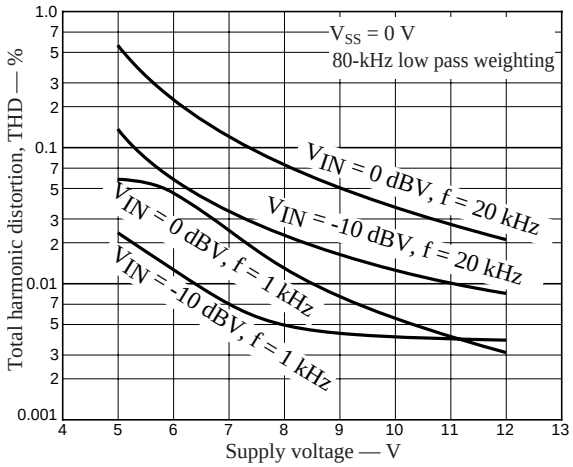


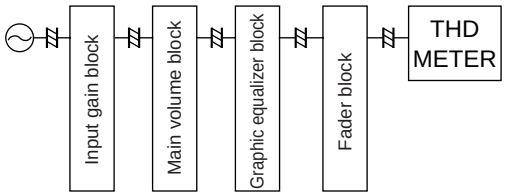


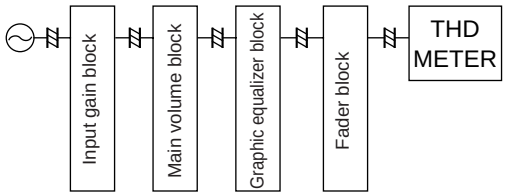
THD – Input Level Characteristics



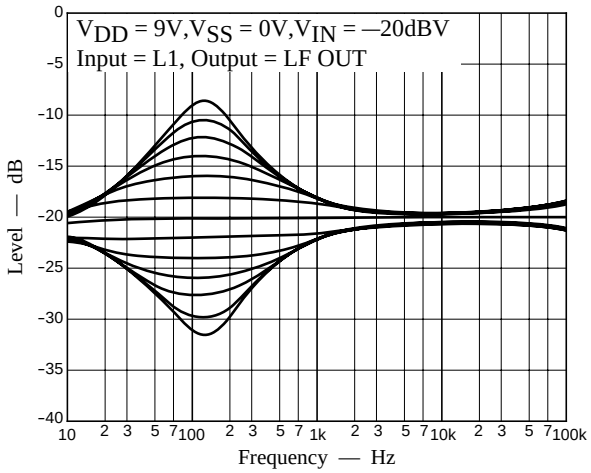
THD – Supply Voltage Characteristics



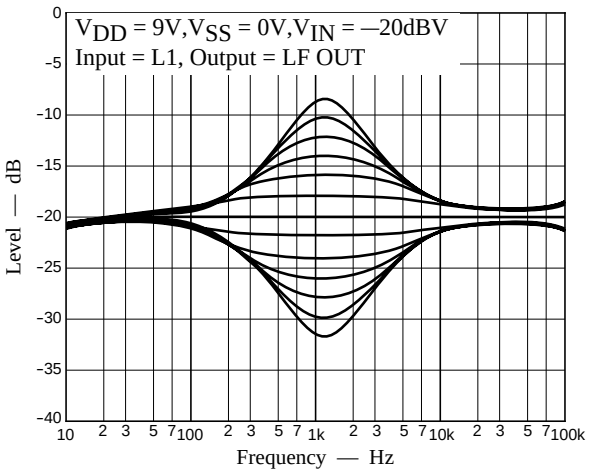




F1 Band Characteristics



F2 Band Characteristics



F3 Band characteristics