FSC-BT806

5.0 Dual Mode Bluetooth Module Datasheet

Version 1.0

Revision History

Version	Data	Notes	
1.0	2018/05/25	Initial Version	Devin Wan

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1. INTRODUCTION

Overview

FSC-BT806 is a Bluetooth 4.0 dual-mode module (Software complies with the Bluetooth Core v5.0 Specification). It provides a Bluetooth Low Energy fully compliant system for audio and data communication with Feasycom stack.

FSC-BT806 integrates an ultra-low-power DSP and application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, I^2S, LED drivers and ADC I/O in a SOC IC. The dual-core architecture with flash memory enables manufacturers to easily differentiate their products with new features without extending development cycles.

By default, FSC-BT806 module is equipped with powerful and easy-to-use Feasycom firmware. It's easy-to-use and completely encapsulated. Feasycom firmware enables users to access Bluetooth functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth modem.

Therefore, FSC-BT806 provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their design.

Features

- Bluetooth v5.0/4.0/3.0/2.1/2.0/1.2/1.1, Class 1.5
- 80MHz RISC MCU and 80MIPS Kalimba DSP
- Stereo codec with 2 channels of ADC and up to 4 microphone inputs (includes bias generators and digital microphone support)
- Support for CSR's latest CVC technology for narrow-band and wideband voice connections including wind noise reduction
- Audio interfaces: I^2S/PCM and SPDIF
- Music Enhancements: SBC,MP3,AAC and AAC+,Faststream codec,atpX,5-band EQ,3D stereo separation and so on.
- Support HSP, HFP, A2DP, AVRCP,PBAP,MAP,SPP,BLE profile
- Multipoint support for HFP connection to 2 handsets for voice
- Multipoint support for A2DP connection to 2 A2DP source for music playback
- 3 Hardware LED controllers(for RGB)
- UART,I^2C,SPI,PIO,AIO,USB control interfaces
- Postage stamp sized form factor
- MFI Support
- Built-in RF combo filter, Built-in PCB antenna to support external antenna
- Fast charging support up to 200mA with no external components
- RoHS compliant
- Industrial temperature range from -40°C to +85°C

Application

- Smart watches & Bluetooth bracelets
- Bluetooth headphones
- Smart remote controllers
- Wired or wireless sound bars
- Wired or wireless speakers
- Wearable audio with sensors(health and well-being applications)
- Stereo (AV) Transmitter

- Automotive Hands-Free Kits

Module picture as below showing

Figure 1: FSC-BT806 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	On-board chip	CSR8670/CSR8675
	Bluetooth Low energy	V5.0 Dual-mode Bluetooth low energy radio
		Software complies with the Bluetooth Core v5.0 Specification
		Support for Bluetooth basic rate / EDR and low energy Connections
		3 Bluetooth low energy connections at the same time as basic rate A2DP
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+10 dBm (Maximum)
	Receive Sensitivity	-88 dBm(Typical)
		Real-time digitised RSSI available to application
	Raw Data Rates (Air)	3 Mbps(Classic BT - BR/EDR)
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		8 data bit character
	GPIO	23(maximum – configurable) lines
		O/P drive strength (4 mA)
		Pull-up resistor (33 KΩ) control
		Read pin-level
	I^2C Interface	1 (hardware I^2C interface). Up to 400 kbps Master and slave I^2C interface
	SPI Interface	SPI debug and programming interface with read access disable locking
	ADC Interface	Analog input voltage range: 0~ 1.3V
		Supports single a 10-bit ADC and a 10-bit DAC
		1 channels (configured from GPIO total)
	USB Interface	1 full-speed (12Mbps)
Profiles	BR/EDR	SPP (Serial Port Profile) - Up to 600 Kbps
		A2DP/AVRCP/HFP/HSP/HID/PBAP/SPP Profiles support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
		Simultaneous BR/EDR and BLE support
Maximum Connections	BR/EDR	up to 7 active slaves
	Bluetooth Low Energy	1 connection as peripheral , up to 5 connections as central
FW upgrade		Via UART
		USB
		SPI
Supply Voltage	Supply	VDD_IO: 1.7 ~ 3.6V ; VBAT_IN: 2.8V ~ 4.3V

Power Consumption		Max Peak Current(TX Power @ +10dBm TX): 85mA
		Standby Doze (Wait event) - <1mA (TBD)
		Deep Sleep - ~300uA(TBD)
Physical	Dimensions	13mm(W) X 26.9mm(L) X 2.2mm(H); Pad Pitch 1mm
Environmental	Operating	-40°C to +85°C
	Storage	-40°C to +105°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3 (With JEDEC J-STD-020)
ESD grade:		Human Body Model: Class-2
		Machine Model: Class-200V
		Charged Device Model: Class II

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

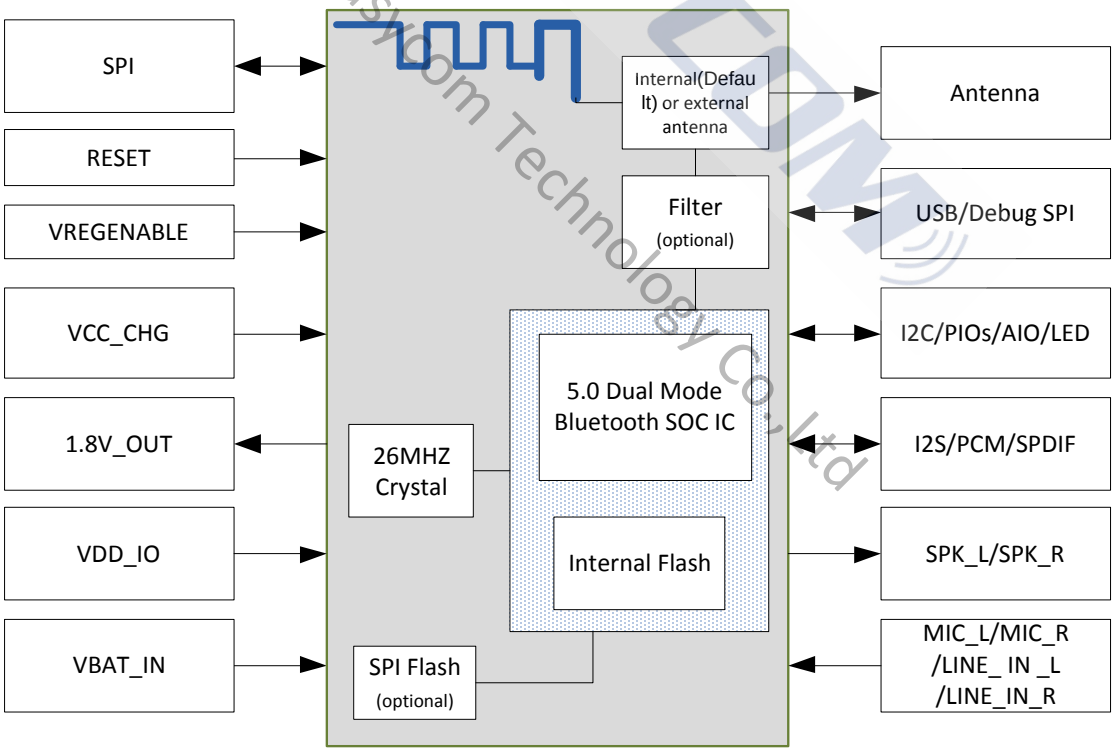


Figure 2: Block Diagram

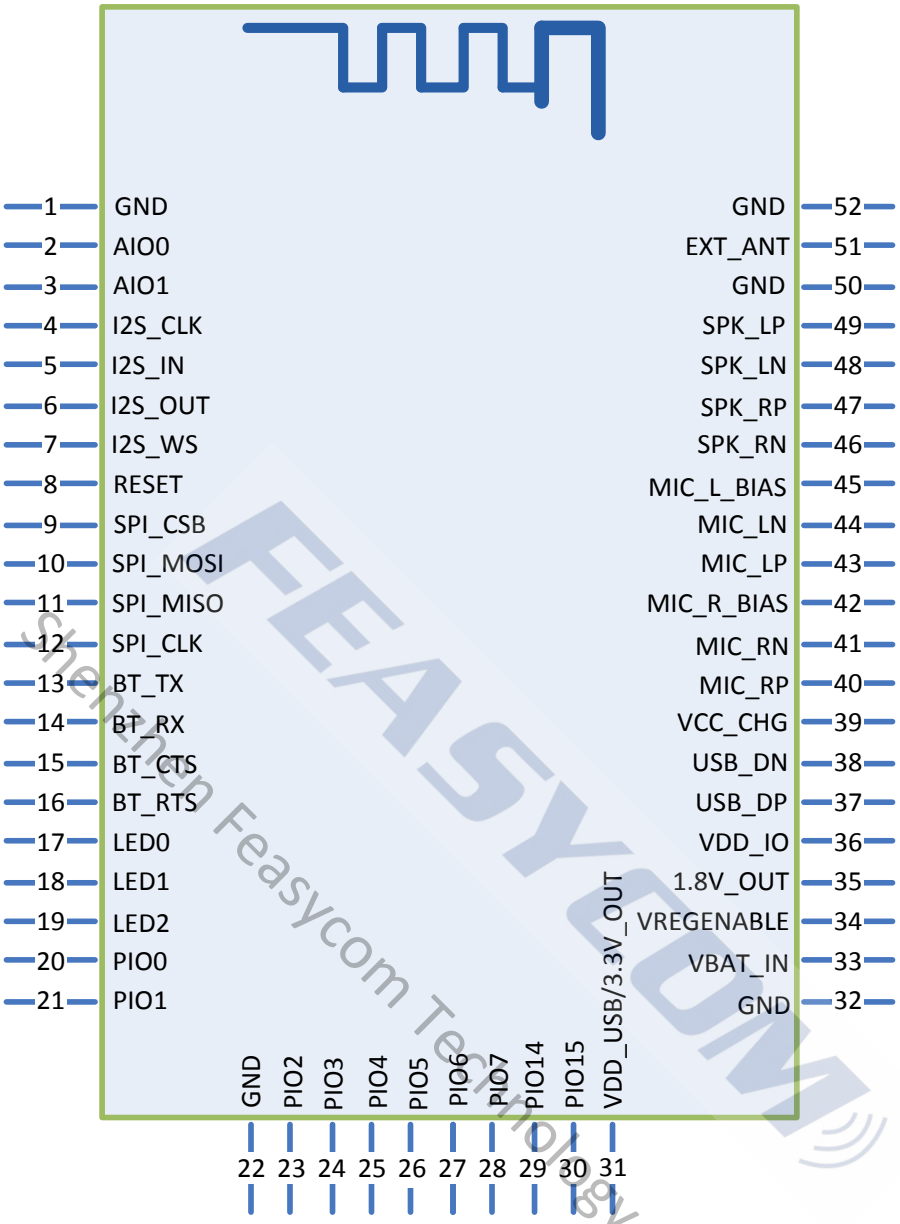


Figure 3: FSC-BT806 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	GND	Vss	Power Ground	
2	AIO0	I/O	Analogue 1 programmable input/output line.	Note 8
3	AIO1	I/O	Analogue 2 programmable input/output line.	Note 8
4	I2S_CLK	I/O	I2S/PCM synchronous data clock. Alternative Function: Programmable input/output line	Note 6
5	I2S_IN	I/O	I2S/PCM synchronous data input. Alternative Function: Programmable input/output line	Note 6
6	I2S_OUT	I/O	I2S/PCM synchronous data output.	Note 6

			Alternative Function: Programmable input/output line	
7	I2S_WS	I/O	I2S/PCM synchronous data sync. Alternative Function: Programmable input/output line	Note 6
8	RESET	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low reset to initial state. (>5mS)	
9	SPI_CSB	I/O	Chip select for SPI, active low.(Debug)	
10	SPI_MOSI	I/O	SPI data input. (Debug)	
11	SPI_MISO	I/O	SPI data output. (Debug)	
12	SPI_CLK	I/O	SPI clock. (Debug)	
13	BT_TX	I/O	UART Data output Alternative Function: Programmable input/output line	Note6
14	BT_RX	I/O	UART Data input Alternative Function: Programmable input/output line	Note 6
15	BT_CTS	I/O	UART clear to send, active low. Alternative Function: Programmable input/output line	Note6
16	BT_RTS	I/O	UART request to send, active low. Alternative Function: Programmable input/output line	Note 6
17	LED0	I/O	LED driver. (RED LED)	Note 6
18	LED1	I/O	LED driver. (BLUE LED)	Note 6
19	LED2	I/O	LED driver. (GREEN LED)	Note 6
20	PIO0	I/O	Programmable input/output line	
21	PIO1	I/O	Programmable input/output line	
22	GND	Vss	Power Ground	
23	PIO2	I/O	Programmable input/output line	
24	PIO3	I/O	Programmable input/output line	
25	PIO4	I/O	Programmable input/output line	
26	PIO5	I/O	Programmable input/output line	
27	PIO6	I/O	Programmable input/output line Alternative Function: I^2C_SCL	Note 5
28	PIO7	I/O	Programmable input/output line Alternative Function: I^2C_SDA	Note 5
29	PIO14	I/O	Programmable input/output line	
30	PIO15	I/O	Programmable input/output line	
31	VDD_USB/3.3V_OUT	Vdd	Positive supply for USB ports/ 3.3V bypass linear regulator output	Note 7
32	GND	Vss	Power Ground	
33	VBAT_IN	Vdd	Power supply voltage 2.8V~ 4.3V (Battery positive terminal)	
34	VREGENABLE	I	Power enable **** The PIN on electricity than VBAT_IN and VDD_IO foot 100 ms delay.***	Note 3
35	1.8V_OUT	Vdd	1.8V switch-mode power regulator output	Note 1
36	VDD_IO	Vdd	Power supply voltage 1.7V ~ 3.6V (for input/output ports)	Note 2
37	USB_DP	I/O	USB data positive	Note 4
38	USB_DN	I/O	USB data negative	Note 4
39	VCC_CHG	Vdd	Battery charger input (5V)	Note 4

40	MIC_RP	I	Microphone input positive, right	
41	MIC_RN	I	Microphone input negative, right	
42	MIC_R_BIAS	O	Microphone R bias	
43	MIC_LP	I	Microphone input positive, left	
44	MIC_LN	I	Microphone input negative, left	
45	MIC_L_BIAS	O	Microphone L bias	
46	SPK_RN	O	Speaker output negative, right	
47	SPK_RP	O	Speaker output positive, right	
48	SPK_LN	O	Speaker output negative, left	
49	SPK_LP	O	Speaker output positive, left	
50	GND	Vss	Power Ground	
51	EXT_ANT	RF	Bluetooth 50Ω transmitter output /receiver input	Note 9
52	GND	Vss	Power Ground	

Module Pin Notes:

Note 1	The internal output of 1.8 V power supply provides maximum 30MA current, and the specific use method can see the application circuit diagram
Note 2	Provid voltage reference to I/O, such as： PIO, UART, SPI, I2S, PCM,etc
Note 3	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input. *** The PIN on electricity than VBAT_IN and VDD_IO foot 100 ms delay.**
Note 4	Using USB function and Lithium battery charging function, the pin should connect 5V voltage
Note 5	I^2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 6	For customized module, this pin can be work as I/O interface.
Note 7	1, When you need to use the USB function, this pin needs to be connected to 3.3V (voltage range: 3.1V~3.6V) 2, when the No. 39 PIN (VCC_CHG) with a 5V input pin, this pin outputs 3.2V ~ 3.4V (maximum current: 250mA)
Note 8	Analog input voltage range: 0~ 1.3V
Note 9	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

4. PHYSICAL INTERFACE

4.1 Power Management

4.1.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.1.2 Battery Charger

4.1.2.1 Battery Charger Hardware Operating Modes

The default mode for the FSC-BT806 battery charger is OFF.

The internal charger circuit can provide up to 200mA of charge current.

The battery charger hardware is controlled by the VM, see picture below. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see the table below and the picture below.

Table 3: Battery Charger Operating Modes Determined by Battery Voltage and Current

Parameter	Battery Charger Enabled	VBAT_SENSE(internal)
Off	No	X
Trickle charge	Yes	>0 and <V_{fast}
Fast charge	Yes	>V_{fast} and <V_{float}
Standby	Yes	I_{term} [(a)] and >(V_{float} - V_{hyst})
Error	Yes	>(VCC_CHG - 50mV)

(a) I_{term} is 10% of I_{fast} for a given I_{fast} setting

The picture below shows the mode-to-mode transition voltages. These voltages are fixed and calibrated. The transition between modes can occur at any time.

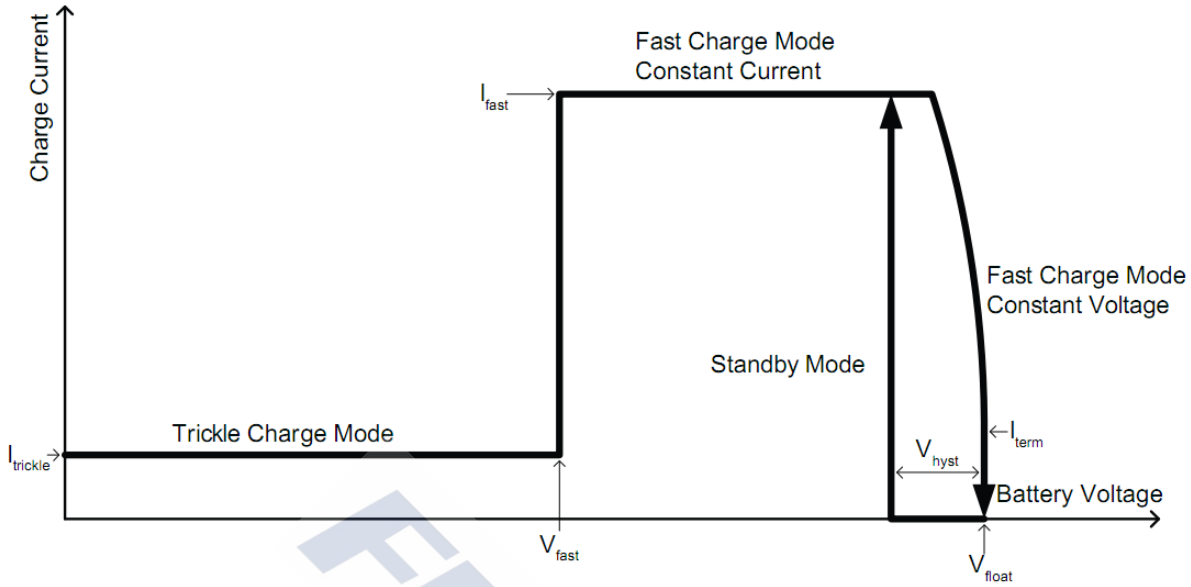


Figure 4: Battery Charger Mode-to-Mode Transition Diagram

Disabled Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the V_{fast} threshold, a current of approximately 10% of the fast charge current, I_{fast}, is sourced from the VBAT_IN pin.

The V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.

Fast Charge Mode

When the voltage on VBAT_SENSE is greater than V_{fast}, the current sourced from the VBAT pin increases to I_{fast}. I_{fast} is between 10mA and 200mA set by PS Key or a VM trap. In addition, I_{fast} is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at I_{fast} until the voltage at VBAT_SENSE reaches V_{float}, then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin.

When the current sourced is below the termination current, I_{term}, the charging stops and the charger enters standby mode. I_{term} is typically 10% of the fast charge current.

Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at V_{hyst} below the final charging voltage, V_{float}, the charger re-enters fast charge mode.

Error Mode

The charger enters the error mode if the voltage on the VCC_CHG pin is too low to operate the charger correctly (VBAT_SENSE is greater than VCC_CHG - 50mV (typical)).

In this mode, charging is stopped. The battery charger does not require a reset to resume normal operation.

4.1.2.2 Battery Charger Trimming and Calibration

The battery charger default trim values are written into internal flash when each IC is characterised. Please contact Feasycom regarding to PS keys.

4.1.2.3 VM Battery Charger Control

The VM charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery
- Monitoring the temperature of the die to protect against silicon damage
- Monitoring the time spent in the various charge states
- Enabling/disabling the charger circuitry based on the monitored information
- Driving the user visible charger status LED(s)

4.1.2.4 Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and call traps from the VM charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys.

4.2 Reset

FSC-BT806 is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. Feasycom recommends applying RST# for a period >5ms.

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate. Following a reset,FSC-BT806 assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until FSC-BT806 is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in FSC-BT806 free runs, again at a safe frequency.

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

4.2.1 Digital Pin States on Reset

This table shows the pin states of FSC-BT806 on reset. PU and PD default to weak values unless specified otherwise.

Table 4: Pin States on Reset

Pin Name/Group	I/O Type	Full Chip Reset
USB_DP	Digital bidirectional	N/A
USB_DN	Digital bidirectional	N/A
BT_TX	Digital bidirectional with PU	Weak PU
BT_RX	Digital bidirectional with PU	Strong PU
BT_CTS	Digital bidirectional with PD	Weak PD
BT_RTS	Digital bidirectional with PU	Strong PU
SPI_CSB	Digital input with PU	Strong PU
SPI_CLK	Digital input with PD	Weak PD
SPI_MISO	Digital tristate output with PD	Weak PD
SPI_MOSI	Digital input with PD	Weak PD
RESET	Digital input with PU	Strong PU
I2S_IN	Digital bidirectional with PD	Weak PD
I2S_OUT	Digital bidirectional with PD	Weak PD
I2S_WS	Digital bidirectional with PD	Weak PD
I2S_CLK	Digital bidirectional with PD	Weak PD
RESET	Digital input with PU	Strong PU
PIO0,1,2,3,4,5,6,7,14,15	Digital bidirectional with PD	Weak PD

4.2.2 Status After Reset

The status of FSC-BT806 after a reset is:

- Warm reset: baud rate and RAM data remain available
- Cold reset: baud rate and RAM data not available

4.2.3 Automatic Reset Protection

FSC-BT806 includes an automatic reset protection circuit which restarts/resets CSR8670 WLCSP when an unexpected reset occurs, e.g. ESD strike or lowering of RST#. The automatic reset protection circuit enables resets from the VM without the requirement for external circuitry.

Note:

The reset protection is cleared after typically 2s (1.6s min to 2.4s max).

If RST# is held low for >2.4s FSC-BT806 turns off.

A rising edge on VREGENABLE or VCC_CHG is required to power on FSC-BT806.

4.3 General Purpose Analog IO

FSC-BT806 has 1 general-purpose analogue interface pins, AIO1, for accessing internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC and a 10-bit DAC. Signals selectable on this interface include the band gap reference voltage. When configured for analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals generated from within the analogue part of the device, the output voltage level is determined by VDD_AUX(internal).

4.4 General Purpose Digital IO

10 lines of programmable bidirectional I/O are available on the FSC-BT806. Some of the PIOs on the FSC-BT806 have alternative functions:

- 3 digital microphone interfaces for control of up to 3 digital microphones:
  - Clock on any even PIOs as determined by the software
  - Data on any odd PIOs as determined by the software
- I²C interface on any PIOs as determined by the software
- LED[2:0] directly map to PO[31:29]
- I2S/PCM interface on PIO[20:17]

4.5 RF Interface

For this module, the antenna must be connected to work properly.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.0 Dual Mode (BT and BLE); 1 Mbps to 3 Mbps over the air data rate.
- TX output power of +10dBm(MAX).
- Receiver to achieve maximum sensitivity -88dBm @ 1 Mbps BLE or Classic BT, 2 Mbps, 3 Mbps).

4.6 Serial Interfaces

4.6.1 UART Interface

FSC-BT806 provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT806 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 5: Possible UART Settings

Parameter		Possible Values
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	4Mbaud(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /2
Bits per channel		8

When connecting the module to a host, please make sure to follow .

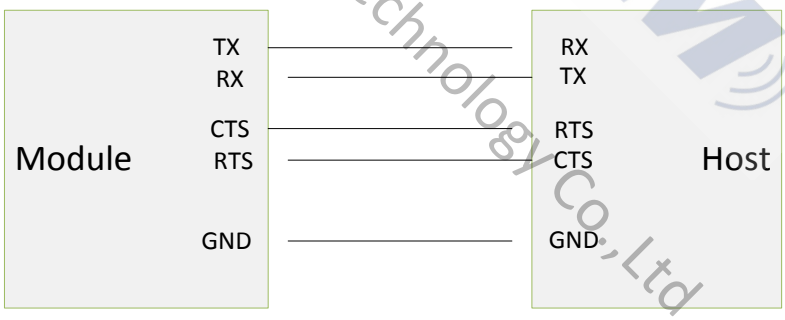


Figure 5: UART Connection

The UART interface resets FSC-BT806 on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as below picture shows. If t BRK is longer than the value defined by the PSKEY_HOSTIO_ UART _RESET_TIMEOUT, a reset occurs. This feature enables a host to initialise the system to a known state. Also, FSC-BT806 can issue a break character for waking the host.

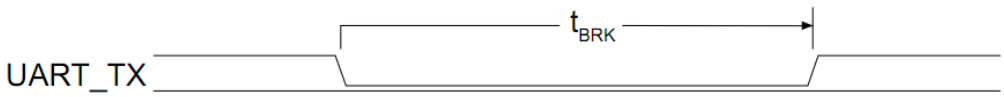


Figure 6: Break Signal

The UART interface is tristate while FSC-BT806 is being held in reset. This enables the user to connect other devices onto the physical UART bus. The restriction with this method is that any devices connected to this bus must tristate when FSC-BT806 reset is de-asserted and the firmware begins to run.

4.6.2 I²C Interface

FSC-BT806 includes a configurable I²C interface.

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I²C Bus Timing.

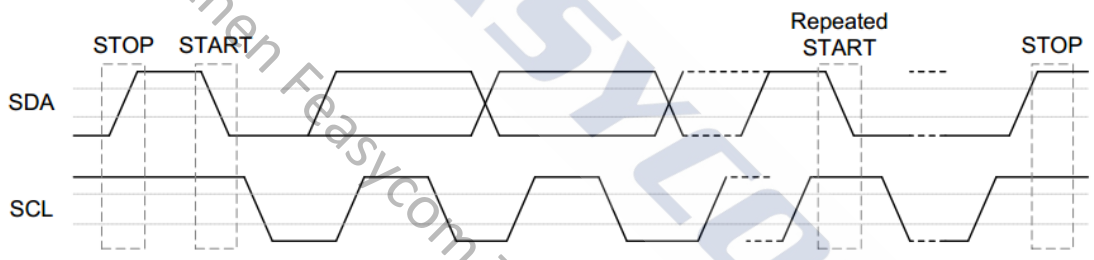


Figure 7: I2C Bus Timing

The device on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

4.6.3 USB Interface

FSC-BT806 has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on FSC-BT806 acts as a USB peripheral, responding to requests from a master host controller.

FSC-BT806 supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification) and USB Battery Charging Specification , available from http://www.usb.org. For more information on how to integrate the USB interface on FSC-BT806 see the Bluetooth and USB Design Considerations Application Note .

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring (when VBUS is>3.1)
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads

- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

4.7 LED Drivers

FSC-BT806 includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in serieswith a current-limiting resistor.

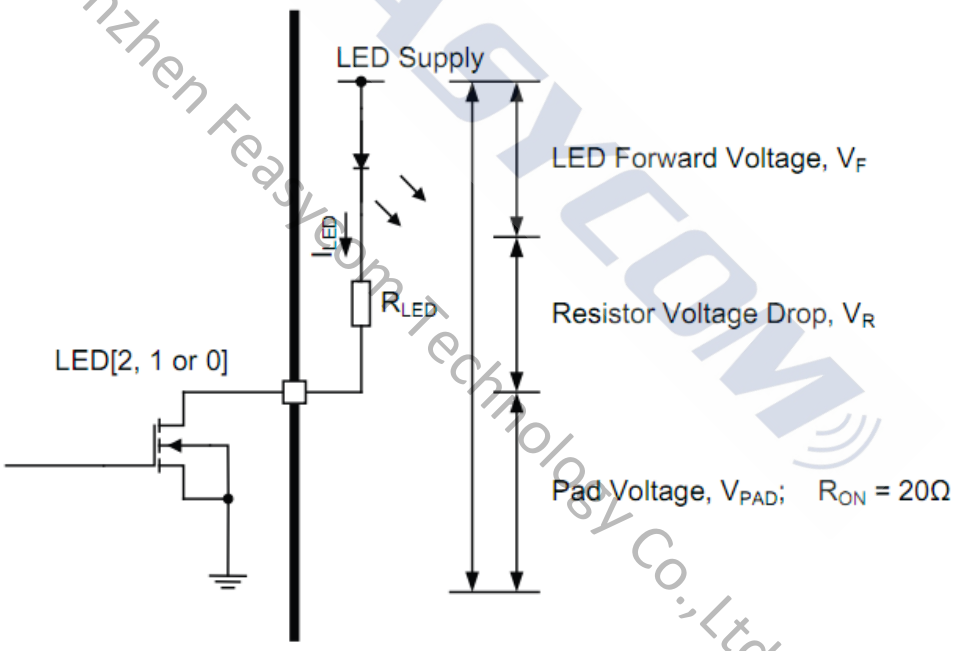


Figure 8: LED Equivalent Circuit

If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED}=\frac{VDD-V_F}{R_{LED}+R_{ON}}$$

For the LED pads to act as resistance, the external series resistor, R_{LED} , needs to be such that the voltage dropacross it, V_R , keeps V_{PAD} below 0.5V.

$$VDD=V_F+V_R+V_{PAD}$$

Note:

The LED current adds to the overall current. Conservative LED selection extends battery life.

4.8 Audio Interfaces

The audio interface circuit consists of:

- Stereo/dual-mono audio codec
- Dual analogue audio inputs
- Dual analogue audio outputs
- 2 digital MEMS microphone inputs
- A configurable PCM, I²S or SPDIF interface

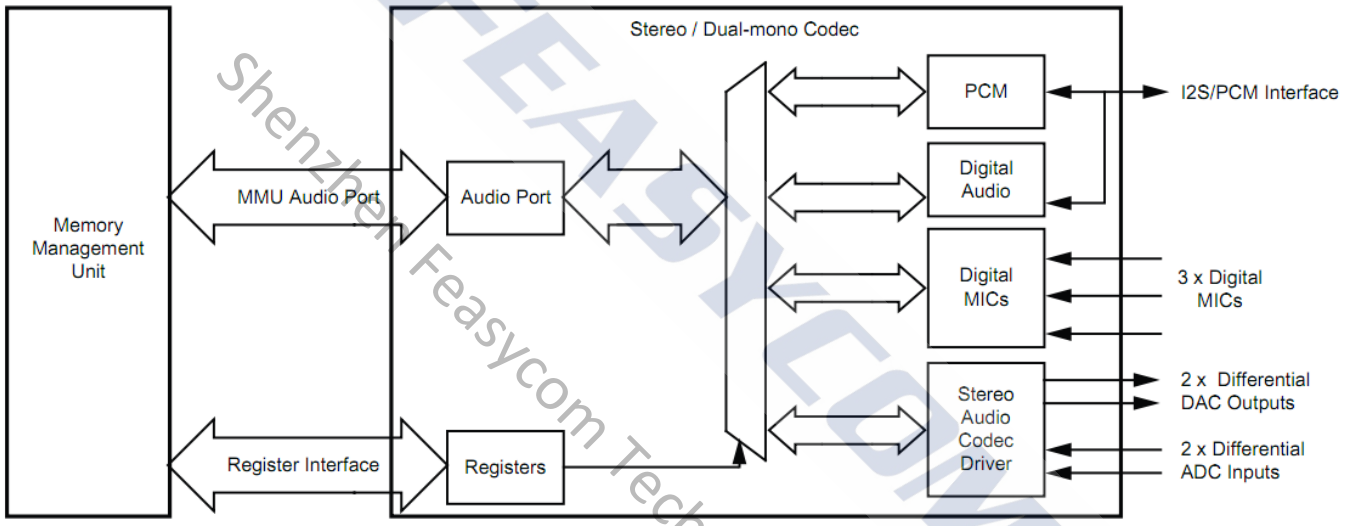


Figure 9: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM codec interface described. which means each of the audio buses are mutually exclusive in their usage.

Table 6: Alternative functions of the digital audio bus interface on the PCM interface

PCM Interface	SPDIF Interface	I2S Interface
PCM_OUT	SPDIF_OUT	I2S_OUT
PCM_IN	SPDIF_IN	I2S_IN
PCM_SYNC		I2S_WS
PCM_CLK		I2S_CLK

4.8.1 Audio Input and Output

The audio input circuitry consists of:

- 2 independent 16-bit high-quality ADC channels:
  - Programmable as either microphone or line input
  - Programmable as either stereo or dual-mono inputs
  - Multiplexed with 2 of the digital microphone inputs
  - Each channel is independently configurable to be either single-ended or fully differential
  - Each channel has an analogue and digital programmable gain stage for optimisation of different microphones
- 2 digital MEMS microphone channels, of which 4 have independent codec channels and 2 share their codecs with the 2 high-quality audio inputs

The audio output circuitry consists of a dual differential class A-B output stage.

Note:

FSC-BT806 is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

4.8.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I²S
- Support for IEC-60958 standard stereo digital audio bus standards, e.g. SPDIF and AES3 (also known as AES/EBU)
- Support for PCM interfaces including PCM master codecs that require an external system clock

Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio output. With respect to audio input, software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel.

Audio Codec Block Diagram

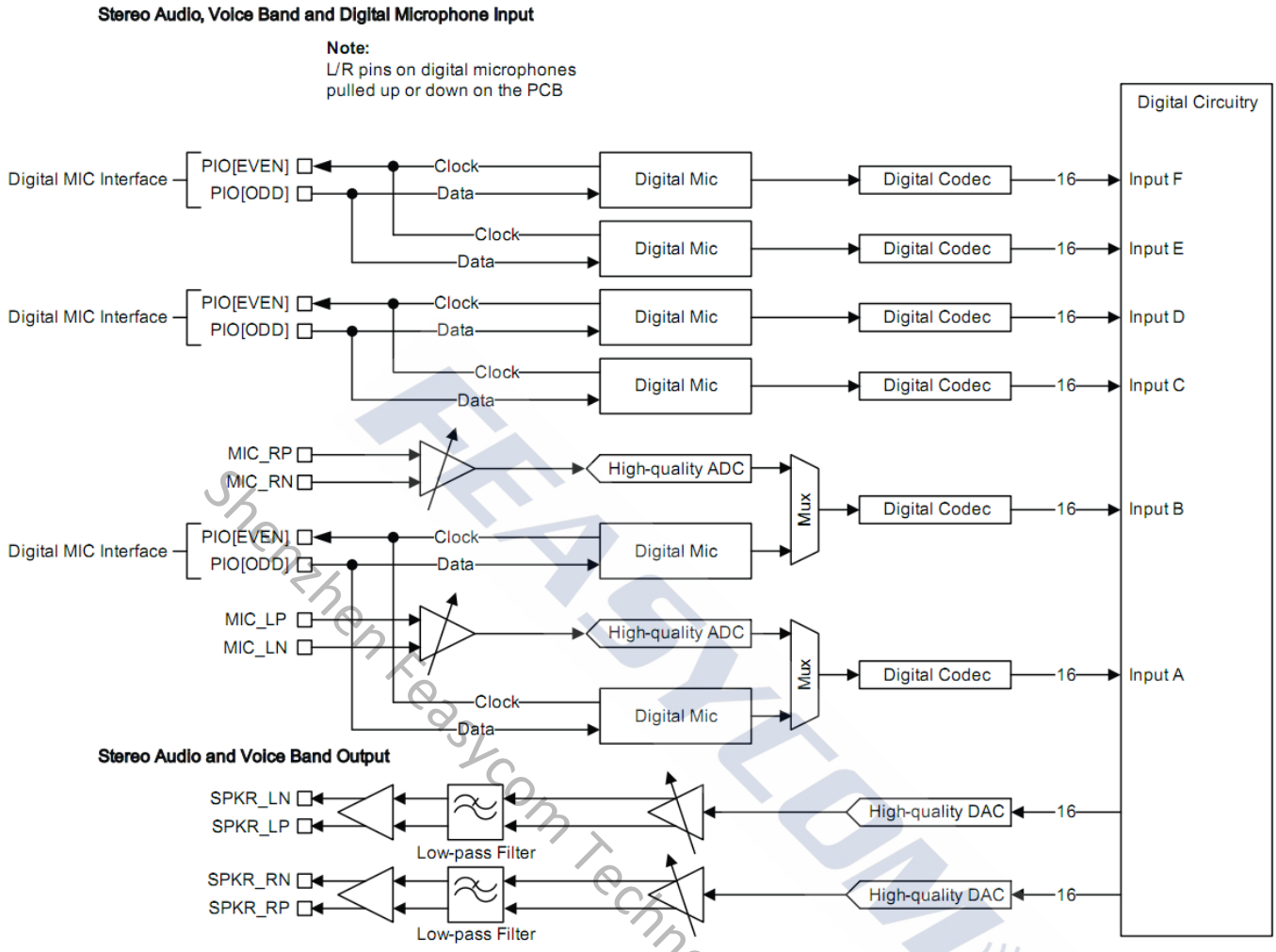


Figure 10: Audio Codec Input and Output Stages

FSC-BT806 audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO(internal) for the audio circuits and VDD_AUDIO_DRV (internal)for the audio driver circuits.

ADC

The picture above shows the FSC-BT806 consists of 2 high-quality ADCs

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is a separate channel with identical functionality.
- There are 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage

ADC Sample Rate Selection

Each ADC supports the following pre-defined sample rates, although other rates are programmable, e.g. 40kHz:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32kHz
- 44.1kHz
- 48kHz

ADC Audio Input Gain

The picture below shows that the FSC-BT806 audio input gain consists of:

- An analogue gain stage based on a pre-amplifier and an analogue gain amplifier
- A digital gain stage

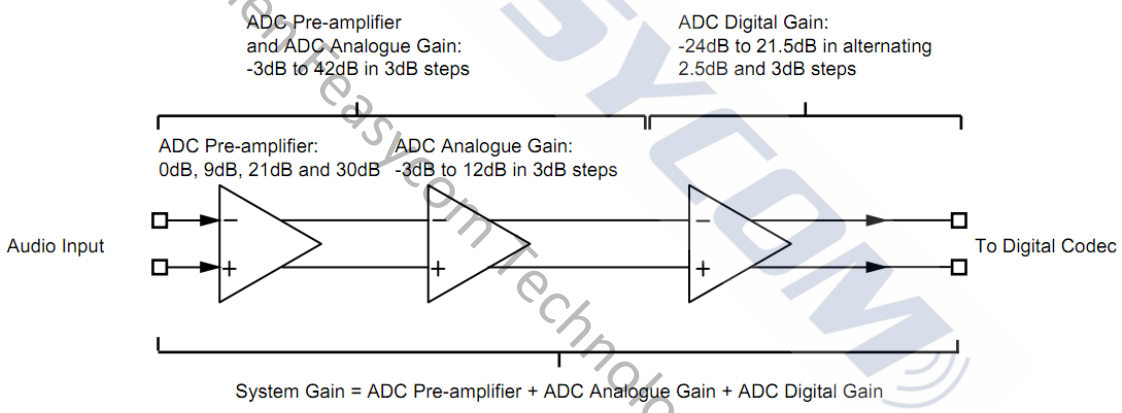


Figure 11: Audio Input Gain

ADC Pre-amplifier and ADC Analogue Gain

FSC-BT806 has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

- The ADC pre-amplifier has 4 gain settings: 0dB, 9dB, 21dB and 30dB
- The ADC analogue amplifier gain is -3dB to 12dB in 3dB steps
- The overall analogue gain for the pre-amplifier and analogue amplifier is -3dB to 42dB in 3dB steps
- At mid to high gain levels it acts as a microphone pre-amplifier
- At low gain levels it acts as an audio line level amplifier

ADC Digital Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB, see following table. There is also a fine gain interface with a 9-bit gain setting allowing gain changes in 1/32 steps, for more infomation contact Feasycom.

The firmware controls the audio input gain.

Table 7: ADC Audio Input Gain Rate

Digital Gain Selection Value	ADC Digital Gain Setting(dB)	Digital Gain Selection Value	ADC Digital Gain Setting(dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

- A long IIR filter suitable for music (>44.1kHz)
- G.722 filter is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance (which is the best selection for 8kHz / 16kHz / voice)

For more information contact Feasycom.

DAC

The DAC consists of:

- 2 fourth-order Sigma-Delta converters enabling 2 separate channels that are identical in functionality
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage.

DAC Sample Rate Selection

Each DAC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 32kHz
- 40kHz
- 44.1kHz
- 48kHz
- 96kHz

DAC Digital Gain

A digital gain stage inside the DAC varies from -24dB to 21.5dB, see following table. There is also a fine gain interface with a 9-bit gain setting enabling gain changes in 1/32 steps, for more information contact CSR.

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

Table 8: DAC Digital Gain Rate Selection

Digital Gain Selection Value	DAC Digital Gain Setting(dB)	Digital Gain Selection Value	DAC Digital Gain Setting(dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

DAC Analogue Gain

The following table shows that the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dBsteps.

The firmware controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

Table 9: DAC Analogue Gain Rate Selection

Analogue Gain Selection Value	DAC Analogue Gain Setting(dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting(dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default long FIR filter for best performance at >= 44.1kHz.
- A short FIR to reduce latency.
- A narrow FIR (a very sharp roll-off at Nyquist) for G.722 compliance. Best for 8kHz / 16kHz.

IEC 60958 Interface

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and enables the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the 2 industry standards:

- AES3 (also known as AES/EBU)
- Sony and Philips interface specification SPDIF

The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4.

The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins. The inputand output stages of the SPDIF pins interface to:

- A 75Ω coaxial cable with an RCA connector
- An optical link that uses Toslink optical components

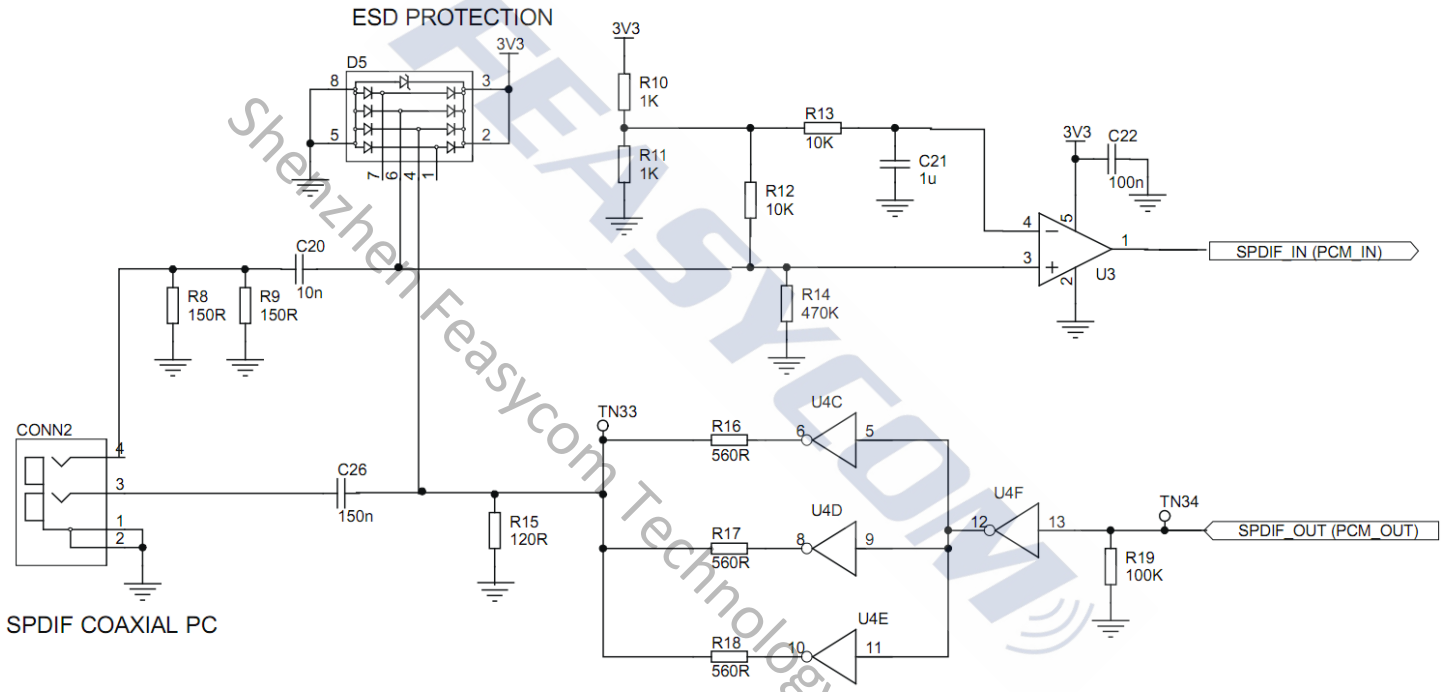


Figure 12: Example Circuit for SPDIF Interface(Co-axial)

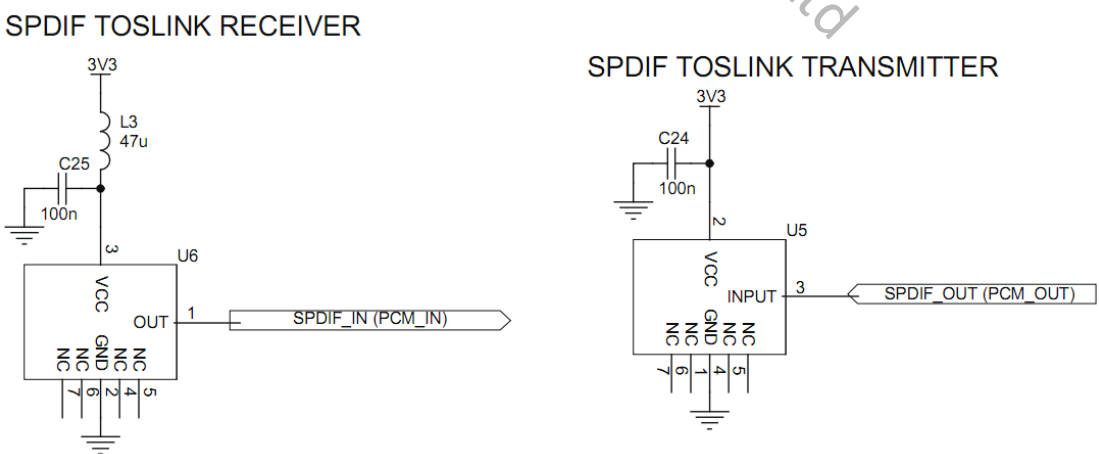


Figure 13: Example Circuit for SPDIF Interface(Optical)

Microphone Input

FSC-BT806 contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones. Figure 9.6 shows a biasing circuit for microphones with a sensitivity between about -40 to -60dB (0dB = 1V/Pa).

Where:

- The microphone bias generator derives its power from VBAT or 3V3_USB and requires no capacitor on its output.
- The microphone bias generator maintains regulation within the limits 70uA to 2.8mA, supporting a 2mA source typically required by 2 electret condensor microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.
- Biasing resistors R1 and R2 equal 2.2kΩ.
- When the input pre-amplifier is enabled, the input impedance at MIC_LN, MIC_LP, MIC_RN and MIC_RP varies between 6kΩ(pre-amplifier gain >0dB) and 12kΩ(pre-amplifier gain = 0dB).
- C1, C2, C3 and C4 are 100/150nF if bass roll-off is required to limit wind noise on the microphone.
- R1 and R2 set the microphone load impedance and are normally around 2.2kΩ.

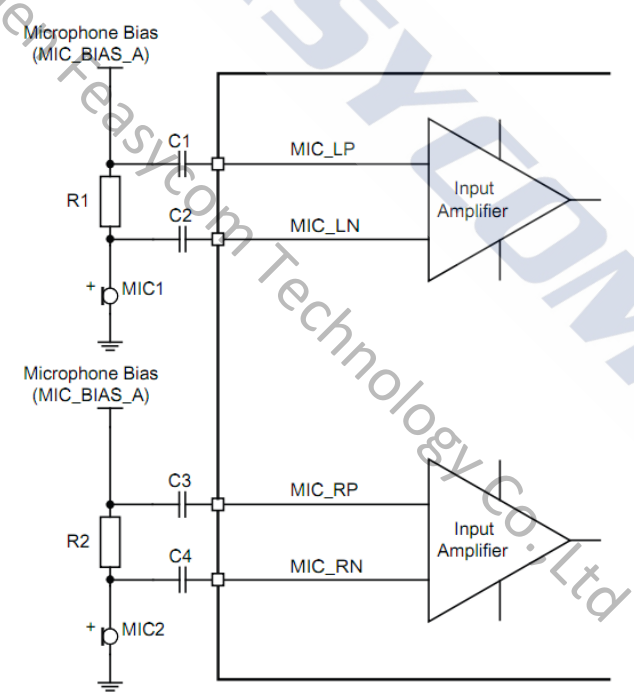


Figure 14: Microphone Biasing

The microphone bias characteristics include:

- Power supply:
  FSC-BT806 microphone supply is VBAT or 3V3_USB(inernal)
  Minimum input voltage = Output voltage + drop-out voltage
  Maximum input voltage is 4.3V
- Drop-out voltage:
  300mV maximum
- Output voltage:

1.8V or 2.6V

Tolerance 90% to 110%

- Output current:

  70uA to 2.8mA

- No load capacitor required

Digital Microphone Inputs

FSC-BT806 interfaces to 2 digital MEMS microphones. shows that 4 of the inputs have dedicated codec channels and 2 are multiplexed with the high-quality ADC channels.

- Clock lines shared between 2 microphone outputs, linked to any even-numbered PIO pin as determinedby the firmware.

  Note:

  Multiple digital microphones can share the same clock if they are configured for the same frequency, e.g. 1 clock for 6 digital microphones.

- Data lines shared between 2 microphone inputs, linked to any odd-numbered PIO as determined by the firmware.

  Note:

  For the digital microphone interface to work in this configuration ensure the microphone uses a tristate between edges.

- The left and right selection for the digital microphones are appropriately pulled up or down for selection on the PCB.

Line Input

The picture below show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

In line input mode, the input impedance of the pins to ground varies from 6kΩ to 34kΩ depending on input gain setting.

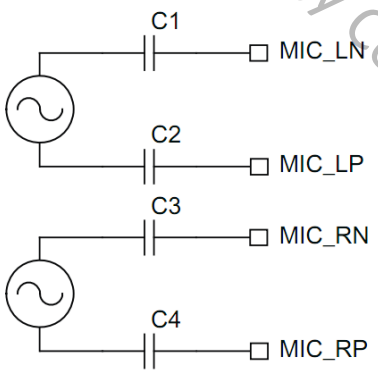


Figure 15: Differential Input

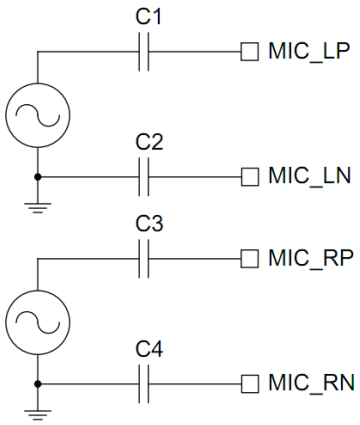


Figure 16: Single-ended Input

4.8.3 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. The picture below shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

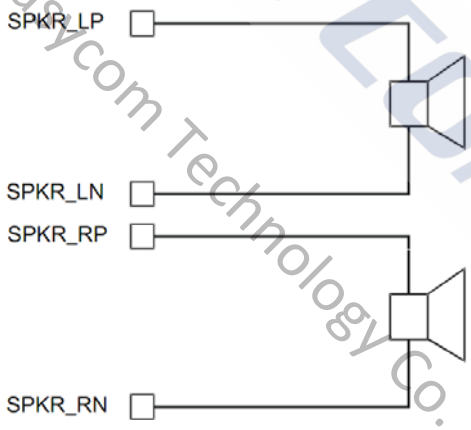


Figure 17: Speaker Output

4.8.4 PCM Controller

The audio PCM interface on the FSC-BT806 supports:

- On-chip routing to Kalimba DSP
- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on the CSR8670 WLCSP for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.

- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
- Long Frame Sync
- Short Frame Sync
- GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

PCM Interface Master/Slave

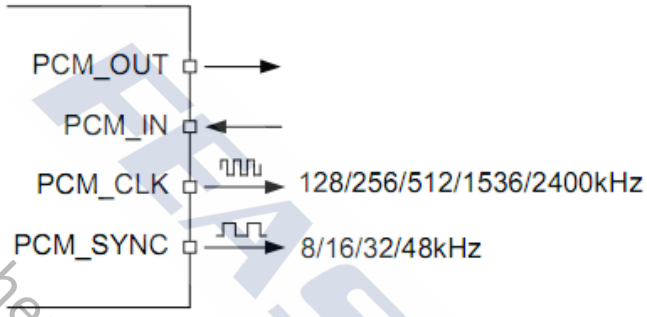


Figure 18: PCM Interface Master

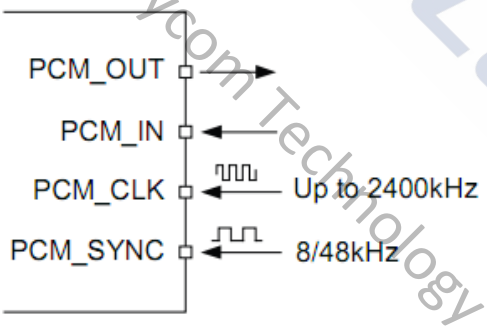


Figure 19: PCM Interface Slave

Long Frame Sync

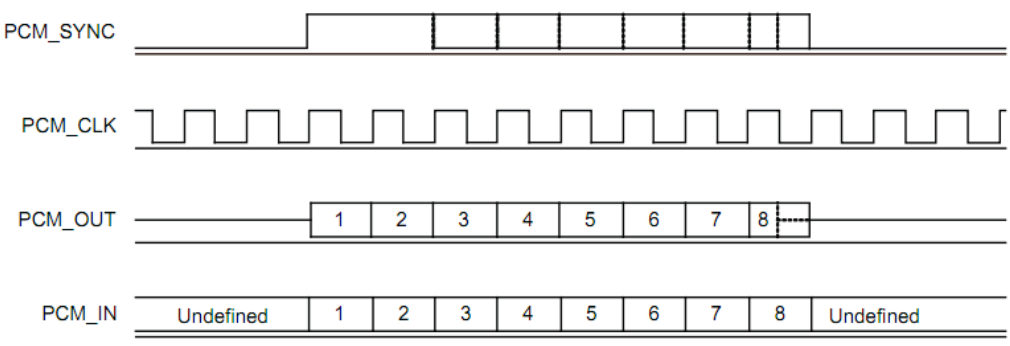


Figure 20: Long Frame Sync (shown with 8-bit Companded Sample)

Short Frame Sync

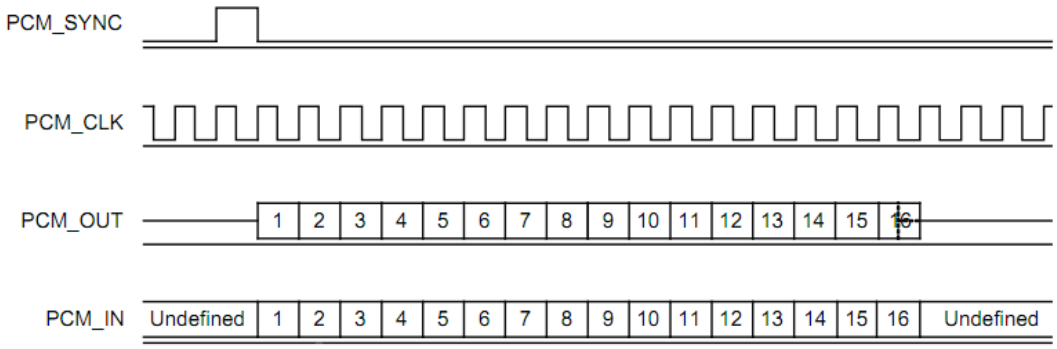


Figure 21: Short Frame Sync (shown with 16-bit Sample)

Multi-slot Operation

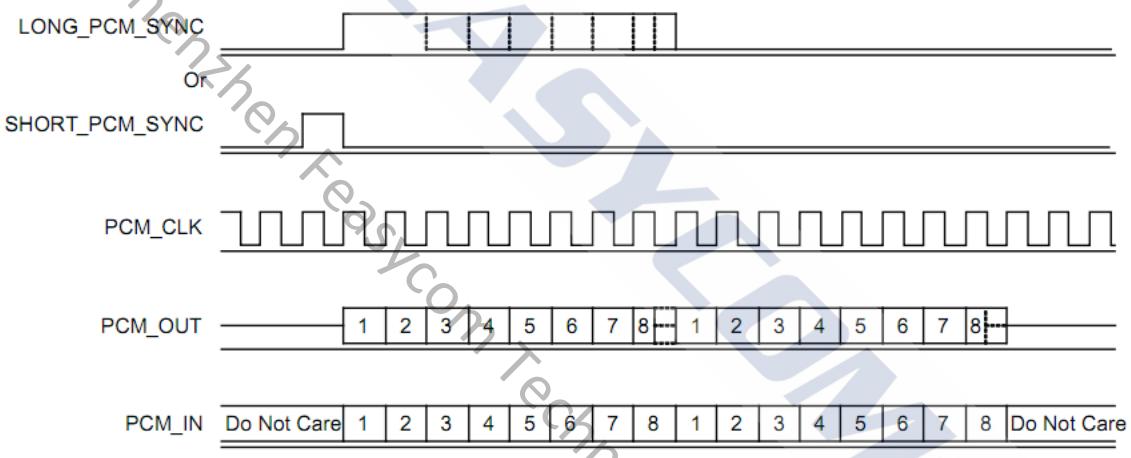


Figure 22: Multi Slot Operation with 2 Slots and 8-bit Companded Samples

GCI Interface

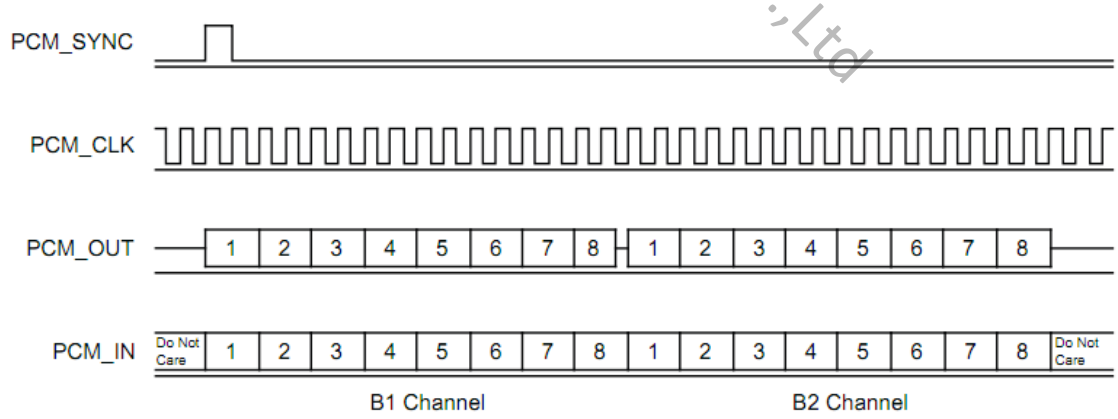


Figure 23: GCI Interface

Slots and Sample Formats

FSC-BT806 receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clocks cycles for 8-bit, 13-bit or 16-bit sample formats.

FSC-BT806 supports:

- 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats.
- A sample rate of 8ksamples/s, 16ksamples/s or 32ksamples/s.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.

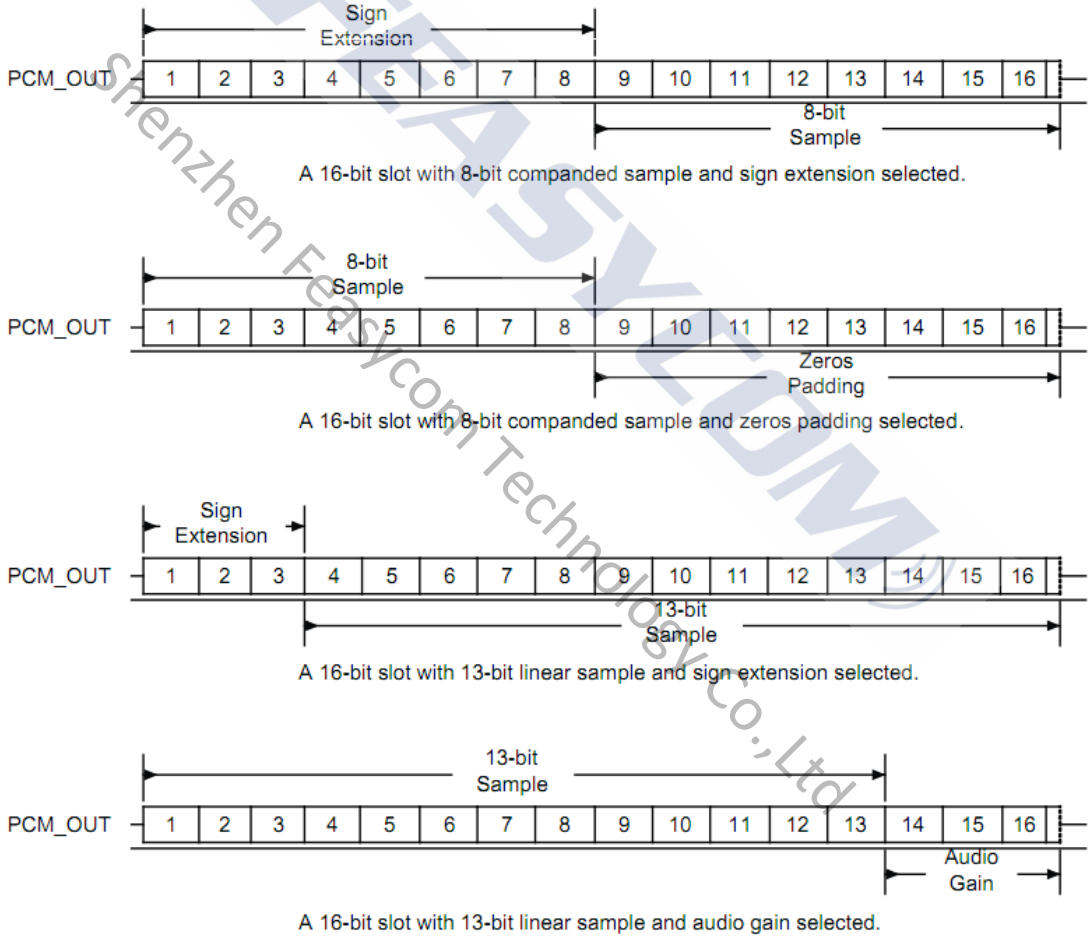


Figure 24: 16-bit Slot Length and Sample Formats

Additional Features

FSC-BT806 has a mute facility that forces PCM_OUT to be 0. In master mode, FSC-BT806 is compatible with some codecs which control power down by forcing PCM_SYNC to 0 while keeping PCM_CLK running.

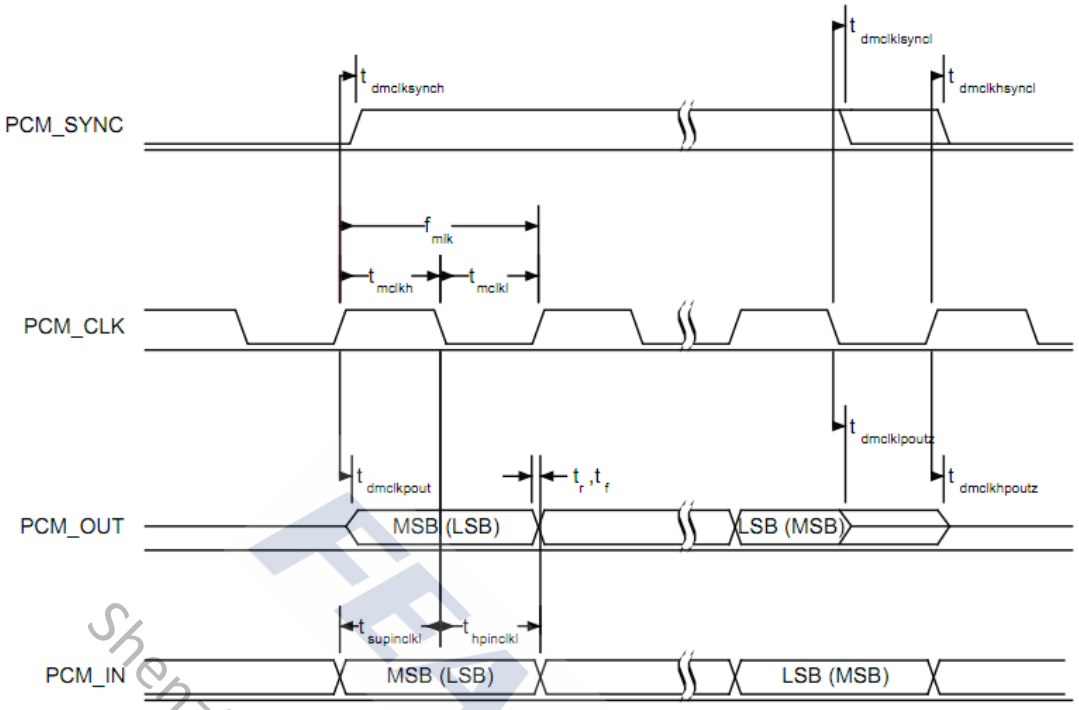


Figure 25: PCM Master Timing Long Frame Sync

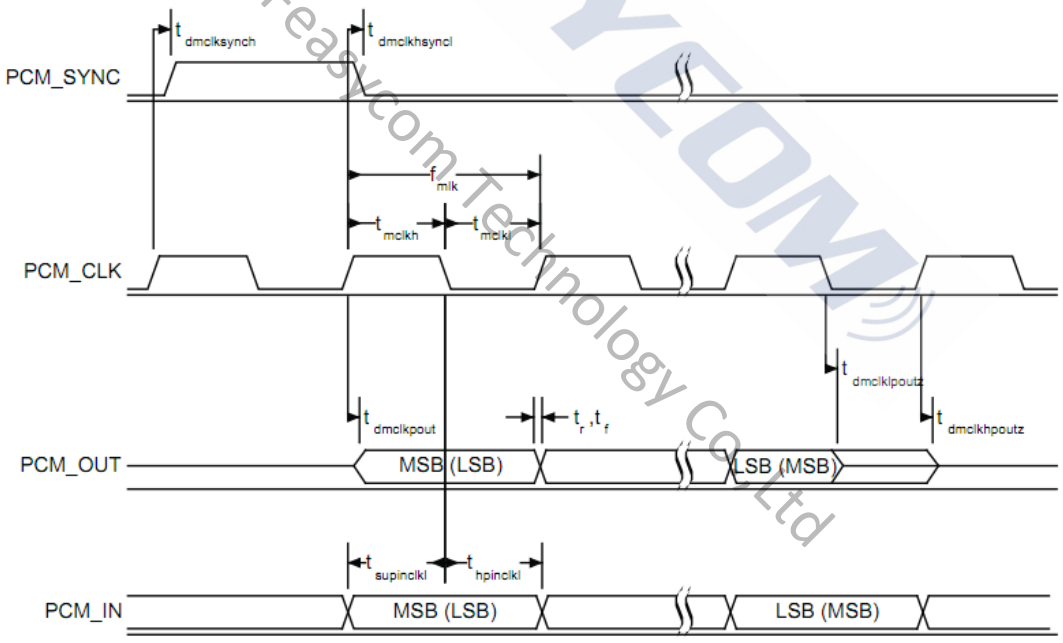


Figure 26: PCM Master Timing Short Frame Sync

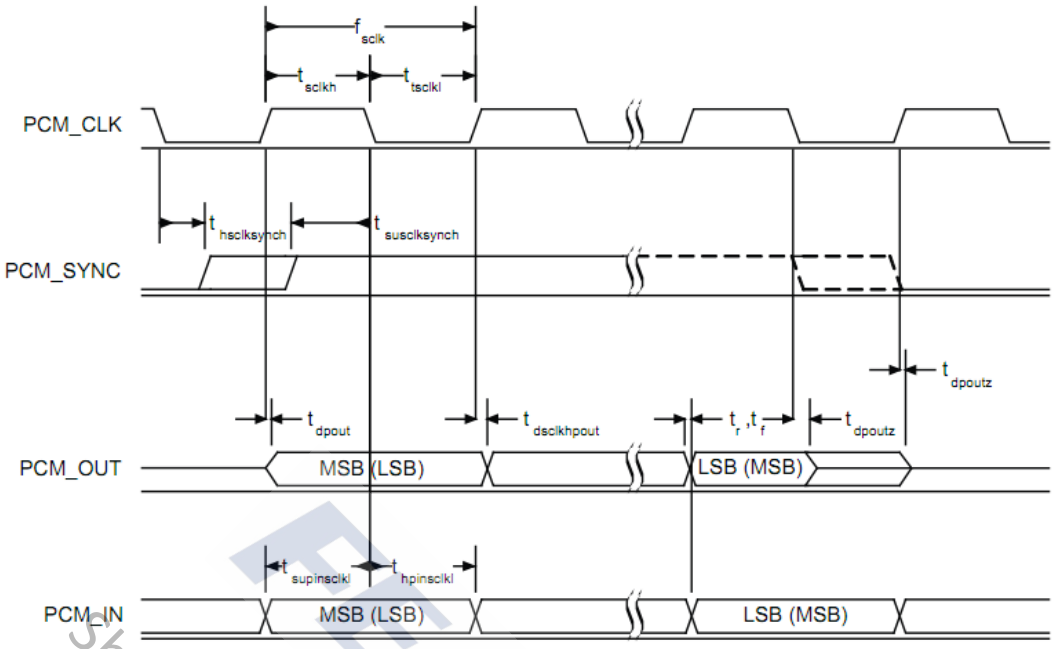


Figure 27: PCM Slave Timing Long Frame Sync

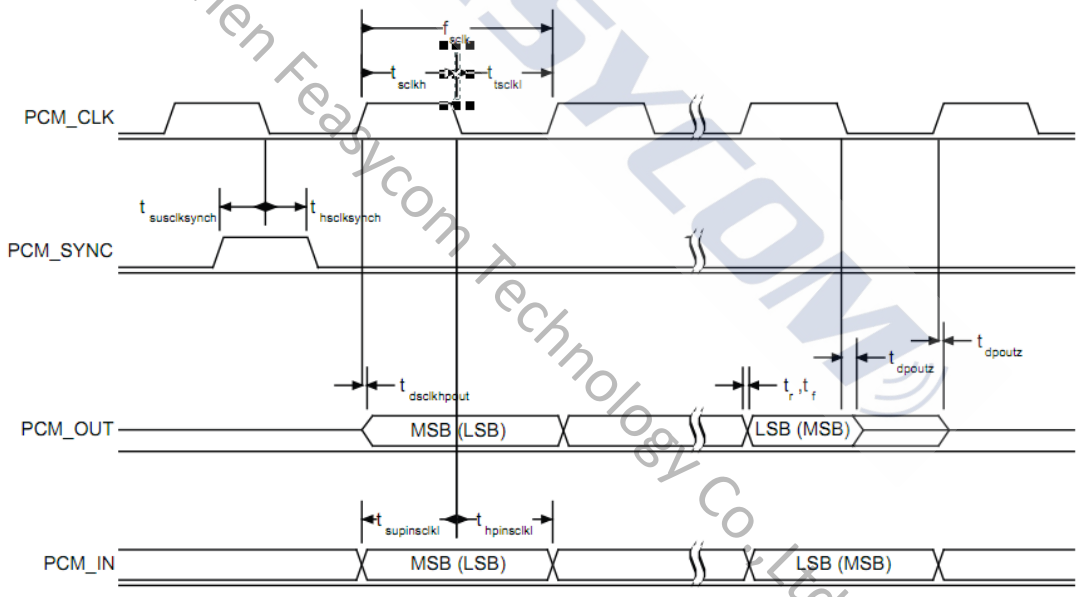


Figure 28: PCM Slave Timing Short Frame Sync

4.8.5 I²S Controller

The digital audio interface supports the industry standard formats for I² S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. This Table lists these alternative functions.

Table 10: Alternative functions of the digital audio bus interface on the PCM interface

PCM Interface	I2S Interface
PCM_OUT	I2S_OUT
PCM_IN	I2S_IN
PCM_SYNC	I2S_WS
PCM_CLK	I2S_CLK

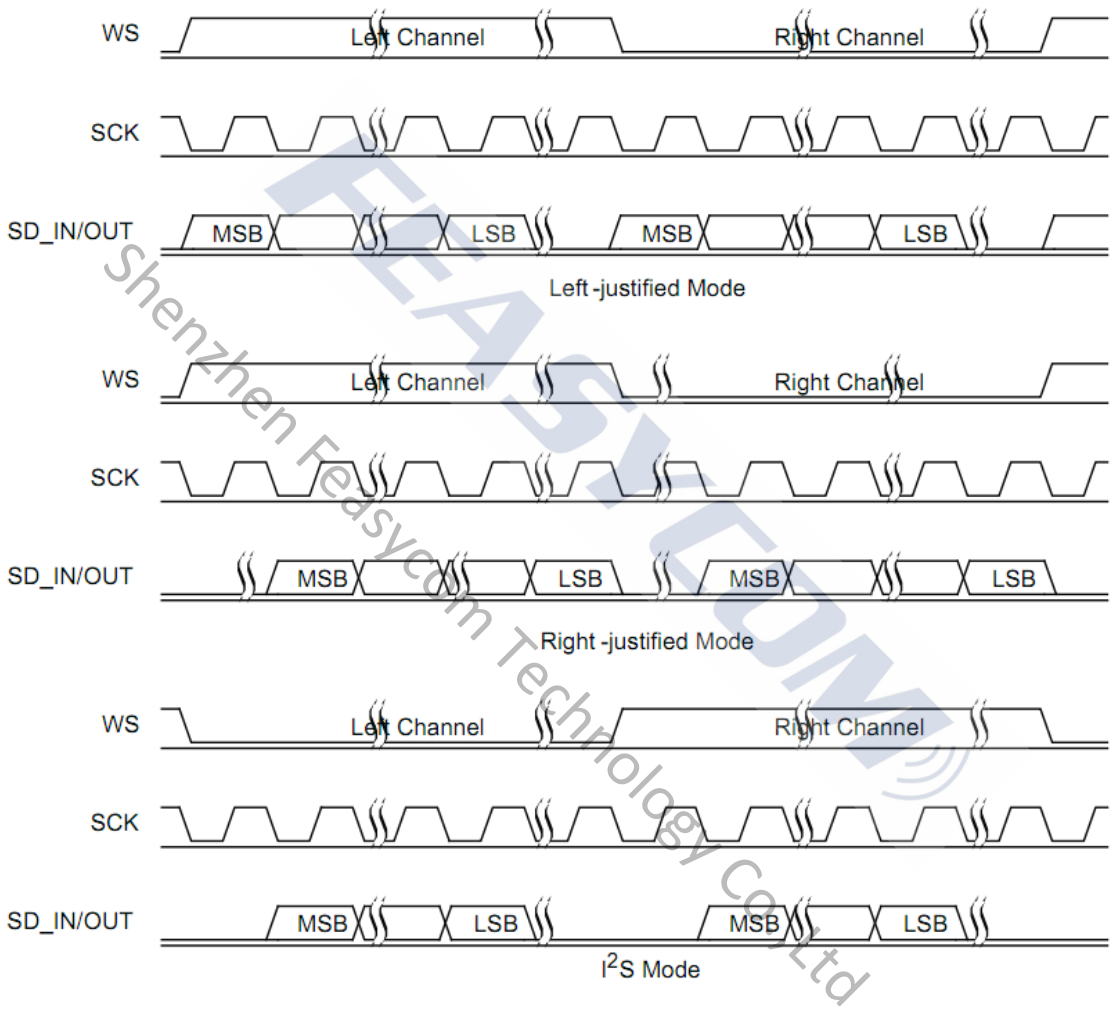


Figure 29： Digital Audio Interface Modes

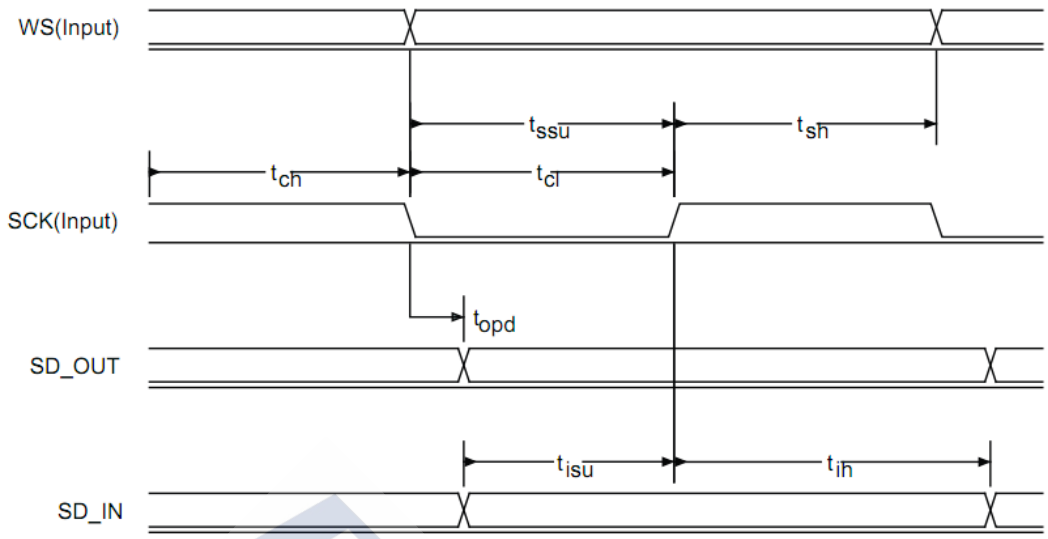


Figure 30： Digital Audio Interface Slave Timing

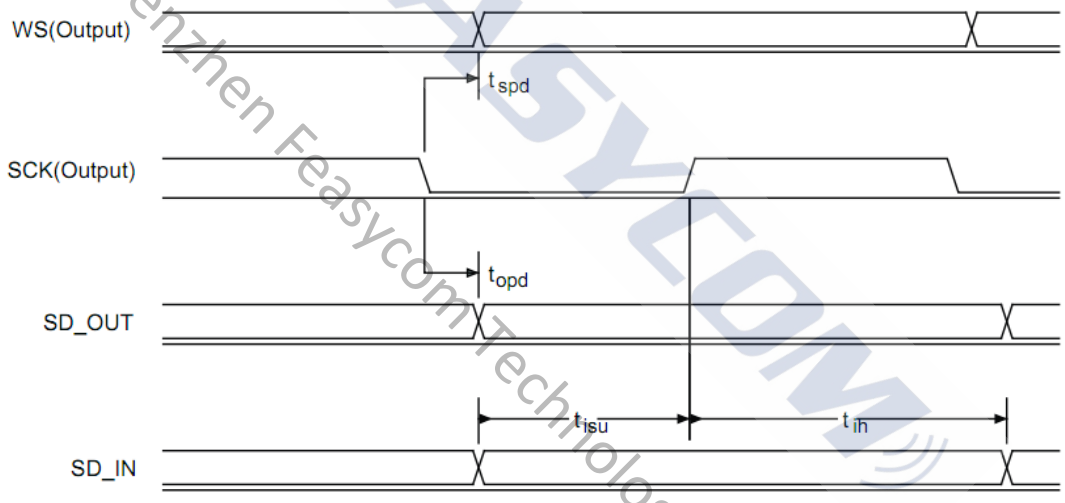


Figure 31： Digital Audio Interface Master Timing

4.9 Programming and Debug Interface

Important Note:

The SPI is for programming, configuring (PS Keys) and debugging the FSC-BT806. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.

Feasycom provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required.

FSC-BT806 uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.
The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 11: Absolute Maximum Rating

Parameter	Min	Max	Unit
5V (VCC_CHG)	-0.4	+ 5.75 / 6.50 [(a)]	V
BATTERY(LED 0,1,2)	-0.4	+4.4	V
BATTERY(VBAT_IN)	2.7	+ 5.75	V
BATTERY(VREGENABLE)	-0.4	+4.4	V
VDD_IO	-0.4	+3.6	V
Other terminal voltages	VSS-0.4	VDD+0.4	V
T_A - Operating Temperature	-40	+85	°C
T_{ST} - Storage Temperature	-40	+105	°C

(a) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.

5.2 Recommended Operating Conditions

Table 12: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
5V (VCC_CHG)	4.75 / 3.10 (a)	5	5.75 / 6.50 (b)	V
BATTERY(LED 0,1,2)	1.10	3.70	4.30	V
BATTERY(VBAT_IN)	2.8	3.3	4.30	V
BATTERY(VREGENABLE)	0	3.3	4.30	V
VDD_IO	1.7	3.3	3.6	V
T_A - Operating Temperature	-40	25	+85	°C
T_{ST} - Storage Temperature	-40	25	+85	°C

(a) Minimum input voltage of 4.75V is required for full specification, regulator operates at reduced load current from 3.1V
(b) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.

5.3 Input/output Terminal Characteristics

5.3.1 Digital

Table 13: DC Characteristics (V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
Input Voltage				
V_{IL} - Standard IO Low level input voltage	-0.4	-	0.4	V
V_{IH} - Standard IO Low level input voltage	0.7XVDD_IO	-	VDD_IO+0.4	V
Tr/Tf	-	-	25	nS
Output Voltage				
V_{OL} - Low Level Output Voltage, I_{OL}=4mA	-	-	0.4	V
V_{OH} - High Level Output Voltage, I_{OH}=-4mA	0.7XVDD_IO	-	-	V
Tr/Tf	-	-	5	nS
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	uA
Strong pull-down	10	40	150	uA
Weak pull-up	-5	-1.0	-0.33	uA
Weak pull-down	0.33	1.0	5.0	uA
C_I Input Capacitance	1.0	-	5.0	pF

5.3.2 Battery Charger

Table 14: Battery Charger

Parameter	Min	Type	Max	Unit
Battery Charger				
Input voltage, VCHG	4.75 / 3.10(a)	5.00	5.75 /6.50(b)	V
(a)Reduced specification from 3.1V to 4.75V. Full specification >4.75V. (b) Standard maximum input voltage is 5.75V, a 6.50V maximum depends on firmware version and implementation of over-temperature protection software, for more information contact Feasycom.				
Trickle Charge Mode				
Charge current $I_{trickle}$, as percentage of fast charge current	8	10	12	%
V_{fast} rising threshold	-	2.9	-	V
V_{fast} rising threshold trim step size	-	0.1	-	V
V_{fast} falling threshold	-	2.8	-	V
Fast Charge Mode				
Charge current during constant current mode, I_{fast} — Max, headroom >0.55V	194	200	206	mA
Charge current during constant current mode, I_{fast} — Min, headroom >0.55V	-	10	-	mA

Reduced headroom charge current,as a percentage of I_{fast}	Mid, headroom =0.15V	50	-	100	%
Charge current step size		-	10	-	mA
V_{float} threshold, calibrated		4.16	4.20	4.24	V
Charge termination current I_{term}, as percentage of I_{fast}		7	10	20	%
Standby Mode					
Voltage hysteresis on VBAT_IN, V_{hyst}		100	-	150	mV
Error Charge Mode					
Headroom(a) error falling threshold		-	50	-	mV
(a) Headroom = VCC_CHG – VBAT_IN					

5.3.3 USB

Table 15: USB

Parameter	Min	Type	Max	Unit
3V3_USB for correct USB operation(internal)	3.10	3.30	3.60	V
Input Threshold				
V_{IL} - input logic level low	-	-	0.3X3V3_USB	V
V_{IH} - input logic level high	0.7X3V3_USB	-	-	V
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} - output logic level low	0	-	0.2	V
V_{OH} - output logic level high	2.8	-	3V3_USB	V

5.3.4 LED Driver Pads

Table 16: LED Driver Pads

Parameter	Min	Type	Max	Unit
Current, I_{PAD} - High impedance state	-	-	5	uA
Current, I_{PAD} - Current sink state	-	-	10	mA
LED pad voltage, V_{PAD} I_{PAD} = 10mA	-	-	0.55	V
LED pad resistance V_{PAD} < 0.5V	-	-	40	Ω

5.4 Stereo Codec

5.4.1 Analogue to Digital Converter

Table 17: Analogue to Digital Converter

Parameter	Ccnditions		Min	Type	Max	Unit
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	48	KHz
SNR	f_{in} = 1kHz B/W = 20Hz->F_{sample} /2 (20kHz max) A-Weighted THD+N < 0.1% 1.6V_{pk-pk} input	F_{sample}				
		8kHz	-	93	-	dB
		16kHz	-	92	-	dB
		32kHz	-	92	-	dB
		44.1kHz	-	92	-	dB
		48kHz	-	92	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz->F_{sample} /2 (20kHz max) 1.6V_{pk-pk} input	F_{sample}				
		8kHz	-	0.004	-	%
		48kHz	-	0.008	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB Analogue setting = -3dB to 12dB in 3dB steps		-3	-	42	dB
Stereo separation (crosstalk)				-89	-	dB

5.4.1 Digital to Analogue Converter

Table 18: Digital to Analogue Converter

Parameter	Ccnditions			Min	Type	Max	Unit
Resolution	-			-	-	16	Bits
Output Sample Rate, F_{sample}	-			8	-	96	KHz
SNR	f_{in} = 1kHz B/W = 20Hz->20KHz A-Weighted THD+N < 0.1% 0dBFS input	F_{sample}	Load				
		48kHz	100KΩ	-	96	-	dB
		48kHz	32Ω	-	96	-	dB
		48kHz	16Ω	-	96	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz->20kHz 0dBFS input	F_{sample}	Load	-			
		8kHz	100KΩ	-	0.002	-	%
		8kHz	32Ω	-	0.002	-	%
		8kHz	16Ω	-	0.003	-	%
		48kHz	100KΩ	-	0.003	-	%

		48kHz	32Ω	-	0.003	-	%
		48kHz	16Ω	-	0.004	-	%
Digital gain	Digital gain resolution = 1/32			-24	-	21.5	dB
Analogue gain	Analogue Gain Resolution = 3dB			-21	-	0	dB
Output voltage	Full-scale swing (differential)			-	-	778	mV rms
Stereo separation (crosstalk)				-	-88	-	dB

5.5 Auxiliary ADC

Table 19: Auxiliary ADC

Parameter		Min	Type	Max	Unit
Resolution		-	-	10	Bits
Input voltage range (a)		0	-	1.8	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DHL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	KHz
Conversion time		1.38	1.69	2.75	uS
Sample rate (b)		-	-	700	Samples/s

(a) LSB size = 1.8V/1023

(b) The auxiliary ADC is accessed through a VM function.The sample rate given is achieved as part of this function.

5.6 Auxiliary DAC

Table 20: Auxiliary DAC

Parameter	Min	Type	Max	Unit
Resolution	-	-	10	Bits
Supply voltage, VDD_AUX	1.30	1.35	1.40	V
Output voltage range	0	-	VDD_AUX	V
Full-scale output voltage	-1	1.35	1.40	V
LSB size	1.30	1.32	2.64	mV
Offset	0	0	1.32	mV
Integral non-linearity	-1.32	0	1	LSB
Settling time (a)	-1	-	250	nS

(a) The settling time does not include any capacitive load

5.7 I²C Dynamic Characteristics

Table 21: I²C Dynamic Characteristics

Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
	Min	Max	Min	Max	
t_{LOW} - SCL low period	4.7	-	1.2	-	uS
T_{HIGH} - SCL high period	4	-	0.6	-	uS
$t_{SU;STA}$ - Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;STA}$ - START condition hold time	4	-	0.6	-	uS
$t_{SU;STO}$ - STOP condition setup time	4	-	0.6	-	uS
t_{BUF} - Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$ - Data setup time	250	-	100	-	uS
$t_{HD;DAT}$ - Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r - SCL/SDA rise time	-	1000	20+0.1CB	300	uS
t_f - SCL/SDA fall time	-	300	-	300	uS
C_b - Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

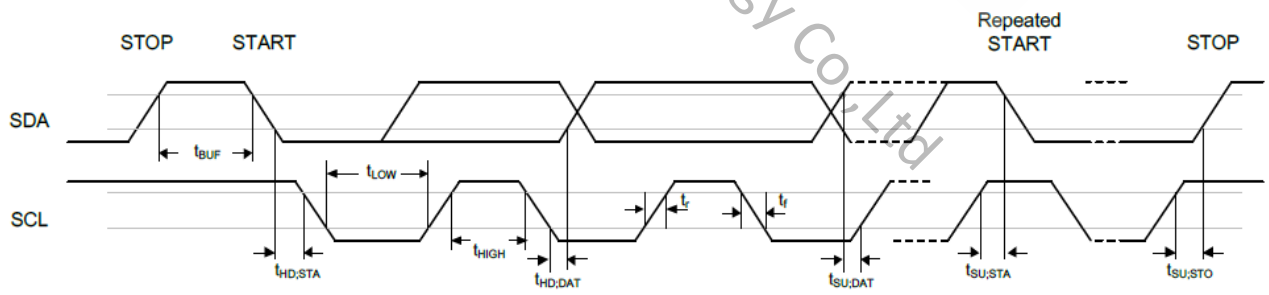


Figure 32: I²C Timing Diagram

5.8 PCM Dynamic Characteristics

Table 22: PCM Dynamic Characteristics

Parameter	Min	Typ	Max	Unit
PCM Master Timing				
f_{mclk} - PCM_CLK frequency 4MHz DDS generation. Selection of frequency is programmable.	-	128 256 512	-	KHz
f_{mclk} - PCM_CLK frequency 48MHz DDS generation. Selection of frequency is programmable.	2.9	-	-	KHz
PCM_SYNC frequency for SCO connection	-	8	-	KHz
t_{mclkh} (a) - PCM_CLK high 4MHz DDS generation	980	-	-	nS
t_{mclkl} (a) - PCM_CLK low 4MHz DDS generation	730	-	-	nS
PCM_CLK jitter 48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$ - Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	nS
$t_{dmclkpout}$ - Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	nS
$t_{dmclklsyncl}$ - Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)	-	-	20	nS
$t_{dmclkhsyncl}$ - Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	nS
$t_{dmclklpoutz}$ - Delay time from PCM_CLK low to PCM_OUT high impedance	-	-	20	nS
$t_{dmclkhpoutz}$ - Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	nS
$t_{supinclkl}$ - Set-up time for PCM_IN valid to PCM_CLK low	20	-	-	nS
$t_{hpinclkl}$ - Hold time for PCM_CLK low to PCM_IN invalid	0	-	-	nS
(a) Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.				
PCM Slave Timing				
f_{sclk} - PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk} - PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl} - PCM_CLK low time	200	-	-	nS
t_{sclkh} - PCM_CLK high time	200	-	-	nS
$t_{hsclksynch}$ - Hold time from PCM_CLK low to PCM_SYNC high	2	-	-	nS
$t_{susclksynch}$ - Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	nS
t_{dpout} - Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	nS
$t_{dsclkhpout}$ - Delay time from CLK high to PCM_OUT valid data	-	-	15	nS
t_{dpoutz} - Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	15	nS
$t_{supinsclkl}$ - Set-up time for PCM_IN valid to CLK low	20	-	-	nS
$t_{hpinsclkl}$ - Hold time for PCM_CLK low to PCM_IN invalid	2	-	-	nS

5.9 I²S Dynamic Characteristics

Table 23: I²S Dynamic Characteristics

Parameter	Min	Typ	Max	Unit
Digital Audio Interface Slave Timing				
SCK Frequency	-	-	6.2	MHz
WS Frequency	-	-	9.6	KHz
t_{ch} - SCK high time	80	-	-	nS
t_{cl} - SCK low time	80	-	-	nS
I2S Slave Mode Timing				
t_{ssu} - WS valid to SCK high set-up time	20	-	-	nS
t_{sh} - SCK high to WS invalid hold time	2.5	-	-	nS
t_{opd} - SCK low to SD_OUT valid delay time	-	-	20	nS
t_{isu} - SD_IN valid to SCK high set-up time	20	-	-	nS
t_{in} - SCK high to SD_IN invalid hold time	2.5	-	-	nS
Digital Audio Interface Master Timing				
SCK Frequency	-	-	6.2	MHz
WS Frequency	-	-	9.6	KHz
I2S Master Mode Timing Parameters,WS and SCK as Outputs				
t_{spd} - SCK low to WS valid delay time	-	-	39.27	nS
t_{opd} - SCK low to SD_OUT valid delay time	-	-	18.44	nS
t_{isu} - SD_IN valid to SCK high set-up time	18.44	-	-	nS
t_{ih} - SCK high to SD_IN invalid hold time	0	-	-	nS

5.10 Power consumptions

Table 24: Power consumptions

Parameter	Test Conditions	Type	Unit
Bluetooth 2.1 Operation Mode	**Current Consumption, Power supply 3.0V**		
Idle	Power on, discoverable and connectable.	~3.8	mA
Searching	Searching devices	~6.8	mA
Connected Standby	Connected, no data traffic	~3.7	mA
(e)SCO traffic	Handsfree calling	~16	mA
RX/TX active	UART data traffic	~8	mA
Bluetooth 4.0 Operation Mode	**Current Consumption, Power supply 3.0V**		
Advertising	Advertising	~3.8	mA
Connected Standby	Connected, no data traffic	~4.3	mA
RX/TX active	UART data traffic	~3.6	mA

Bluetooth 2.1 Operation Mode	Current Consumption, Power supply 3.3V		
Idle	Power on, discoverable and connectable.	~3.6	mA
Searching	Searching devices	~6.3	mA
Connected Standby	Connected, no data traffic	~3.4	mA
(e)SCO traffic	Handsfree calling	~15	mA
RX/TX active	UART data traffic	~7	mA

Bluetooth 4.0/5.0 Operation Mode	Current Consumption, Power supply 3.3V		
Advertising	Advertising	~3.8	mA
Connected Standby	Connected, no data traffic	~4.0	mA
RX/TX active	UART data traffic	~4.1	mA

6. MSL & ESD Protection

Table 25: MSL and ESD

Parameter	Class	Max Rating
MSL grade(with JEDEC J-STD-020)		MSL 3
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	2kV
Machine Model Contact Discharge per JEDEC/EIA JESD22-A115	200V	200V (all pins)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	II	200V (all pins)

6.1 USB Electrostatic Discharge Immunity

FSC-BT806 has integrated ESD protection on the USB_DP and USB_DN pins as detailed in IEC 61000-4-2.

Table 26: USB Electrostatic Discharge Protection Level

IEC 61000-4-2 Level	ESD Test Voltage (Positive and Negative)	IEC 61000-4-2 Classification	Comments
1	2kV contact / 2kV air	Class 1	Normal performance within specification limits
2	4kV contact / 4kV air	Class 1	Normal performance within specification limits
3	6kV contact / 8kV air	Class 2 or class 3	Temporary degradation or operator intervention required
4	8kV contact / 15kV air	Class 2 or class 3	Temporary degradation or operator intervention required

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 27** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 27**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 27: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

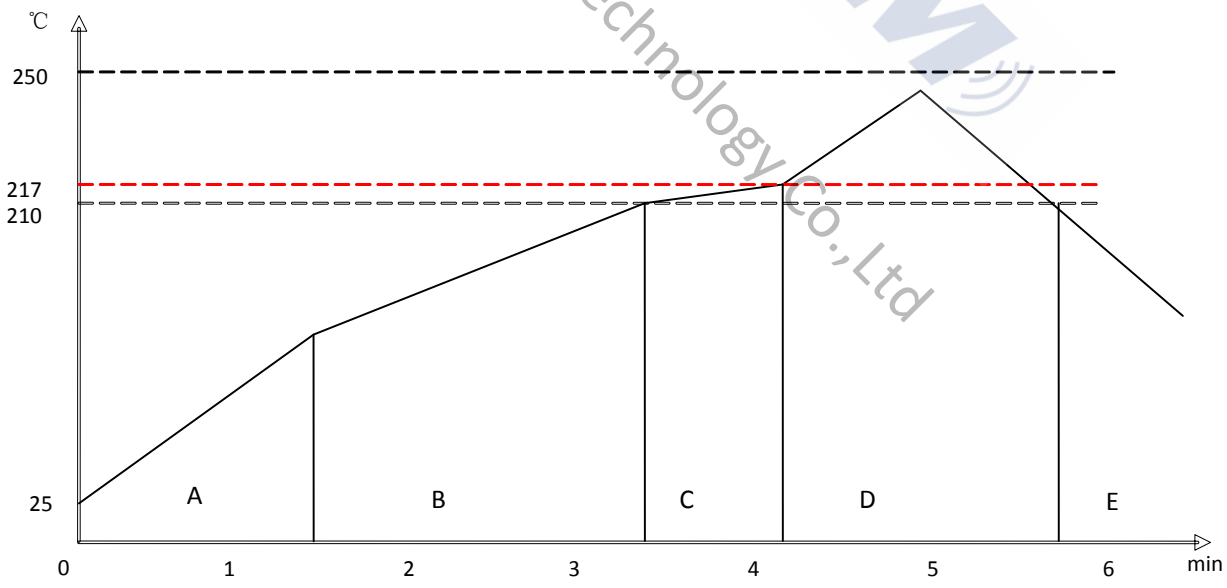


Figure 33: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread

over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.2mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1.6mm X 0.6mm Tolerance: ±0.2mm
- Pad pitch: 1.0mm Tolerance: ±0.1mm

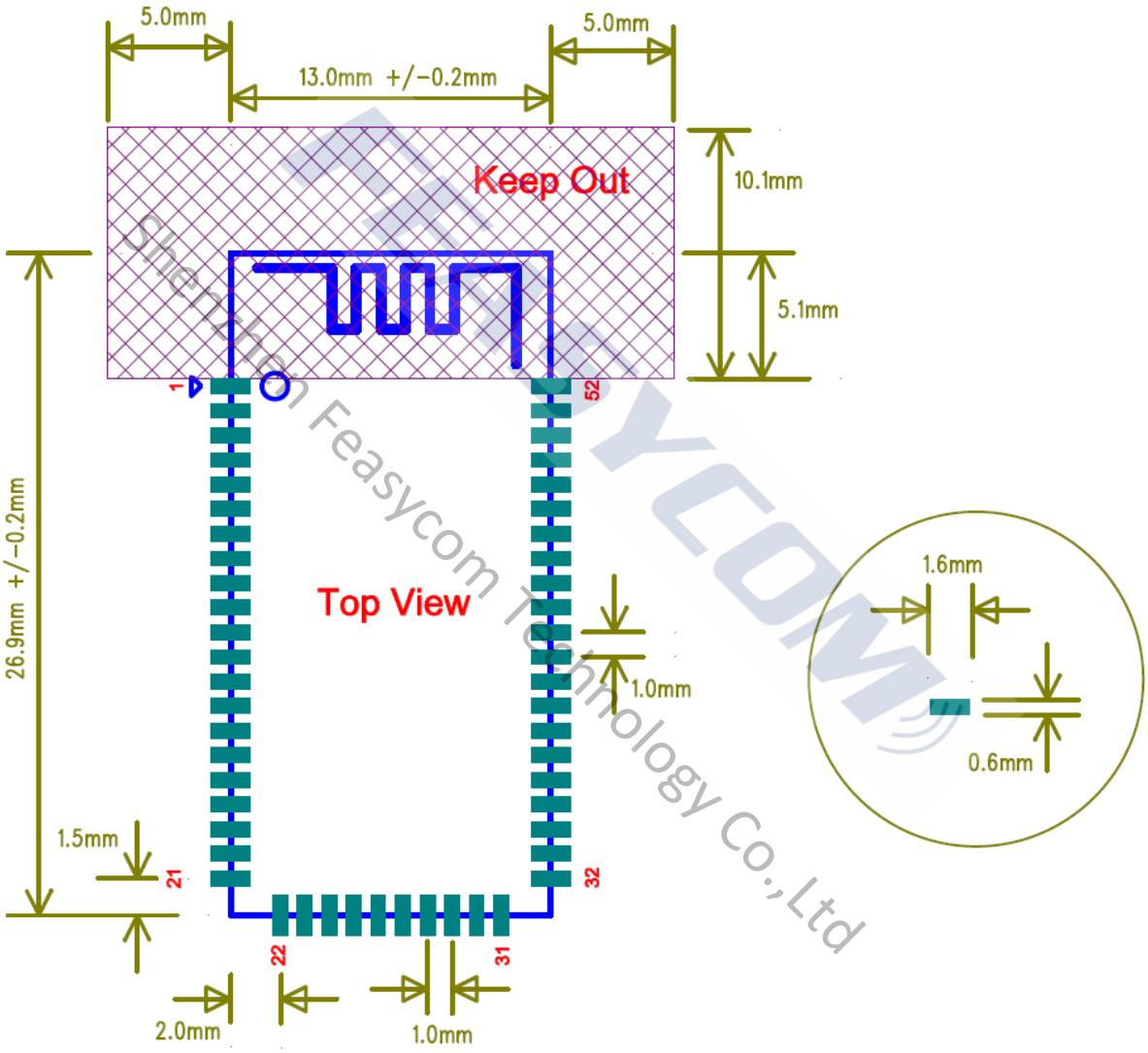


Figure 34: FSC-BT806 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT806 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

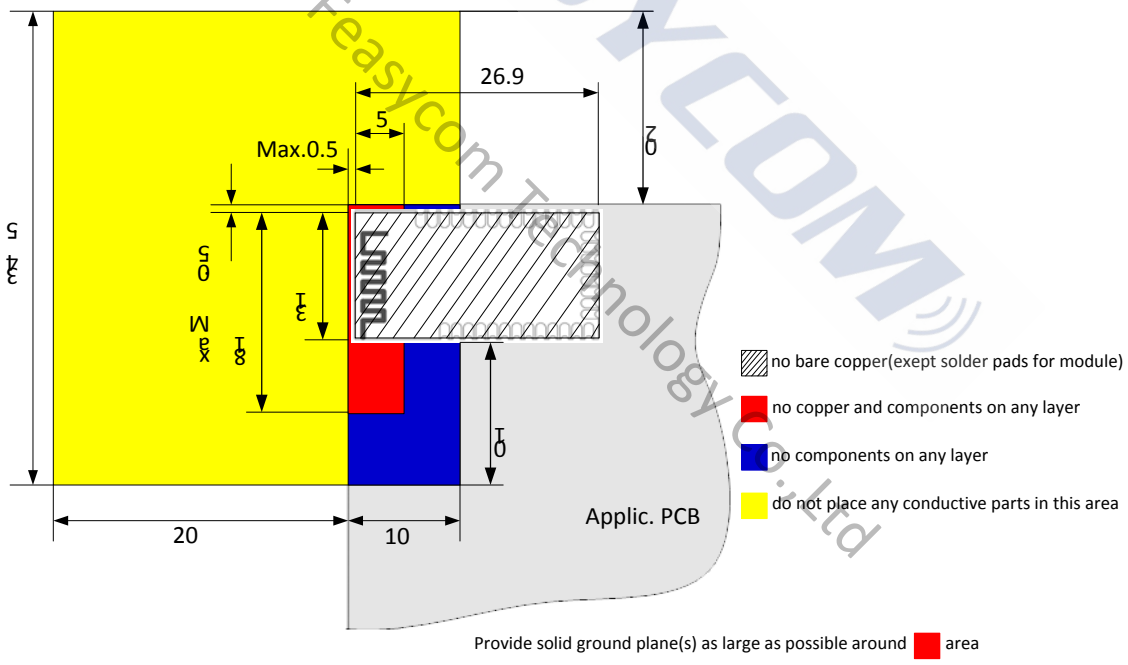


Figure 35: FSC-BT806 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 36** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

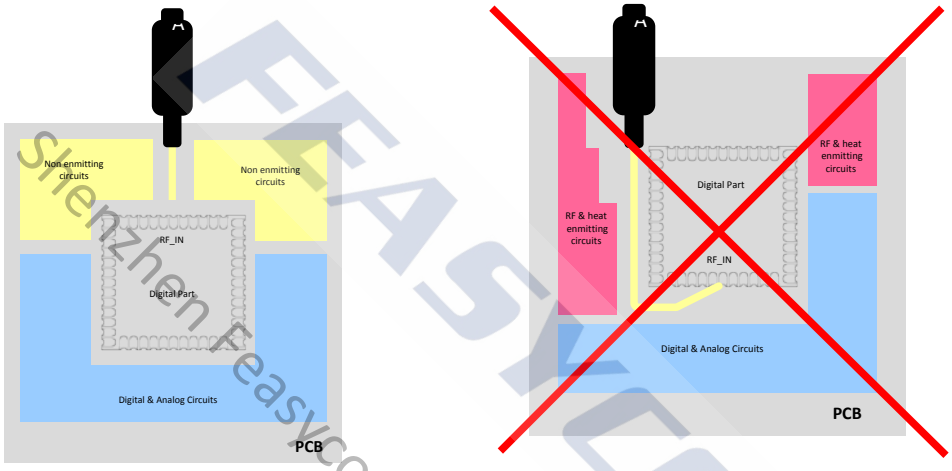


Figure 36: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

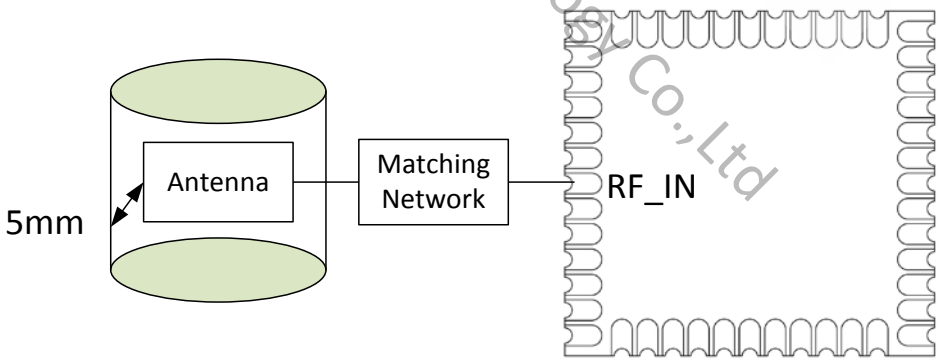


Figure 37: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.

- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

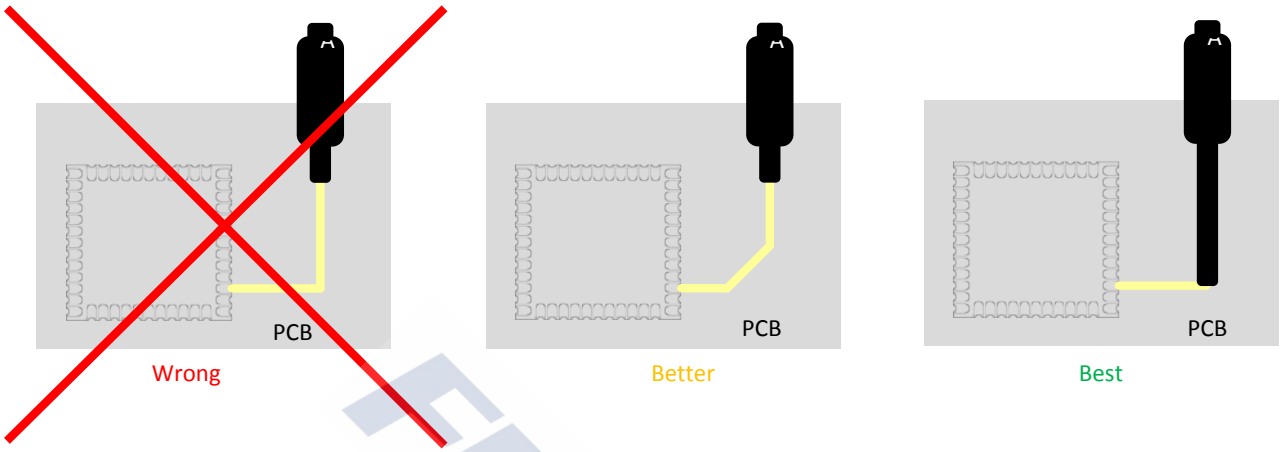


Figure 38: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

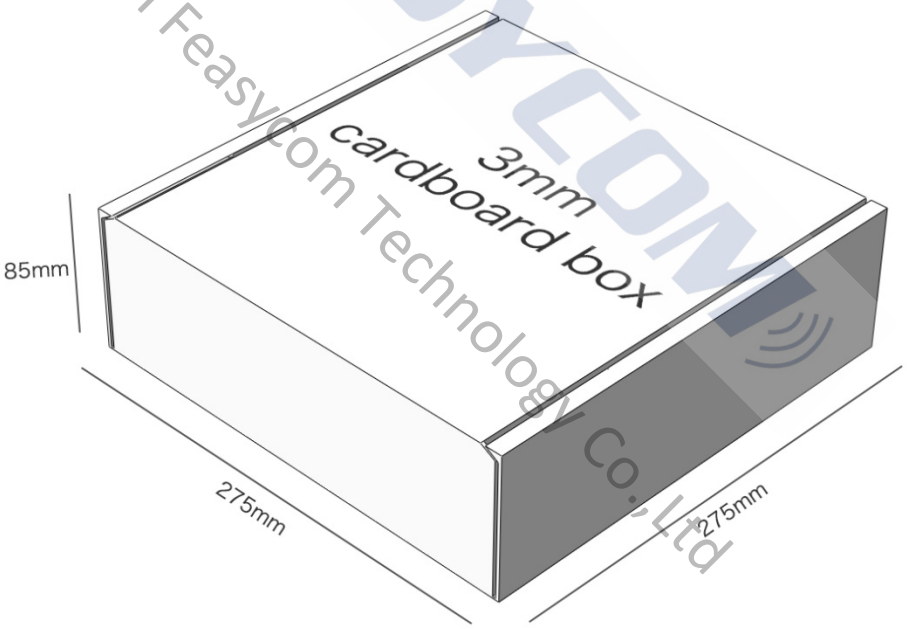
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 39: Tray vacuum

10.2 Packing box(Optional)



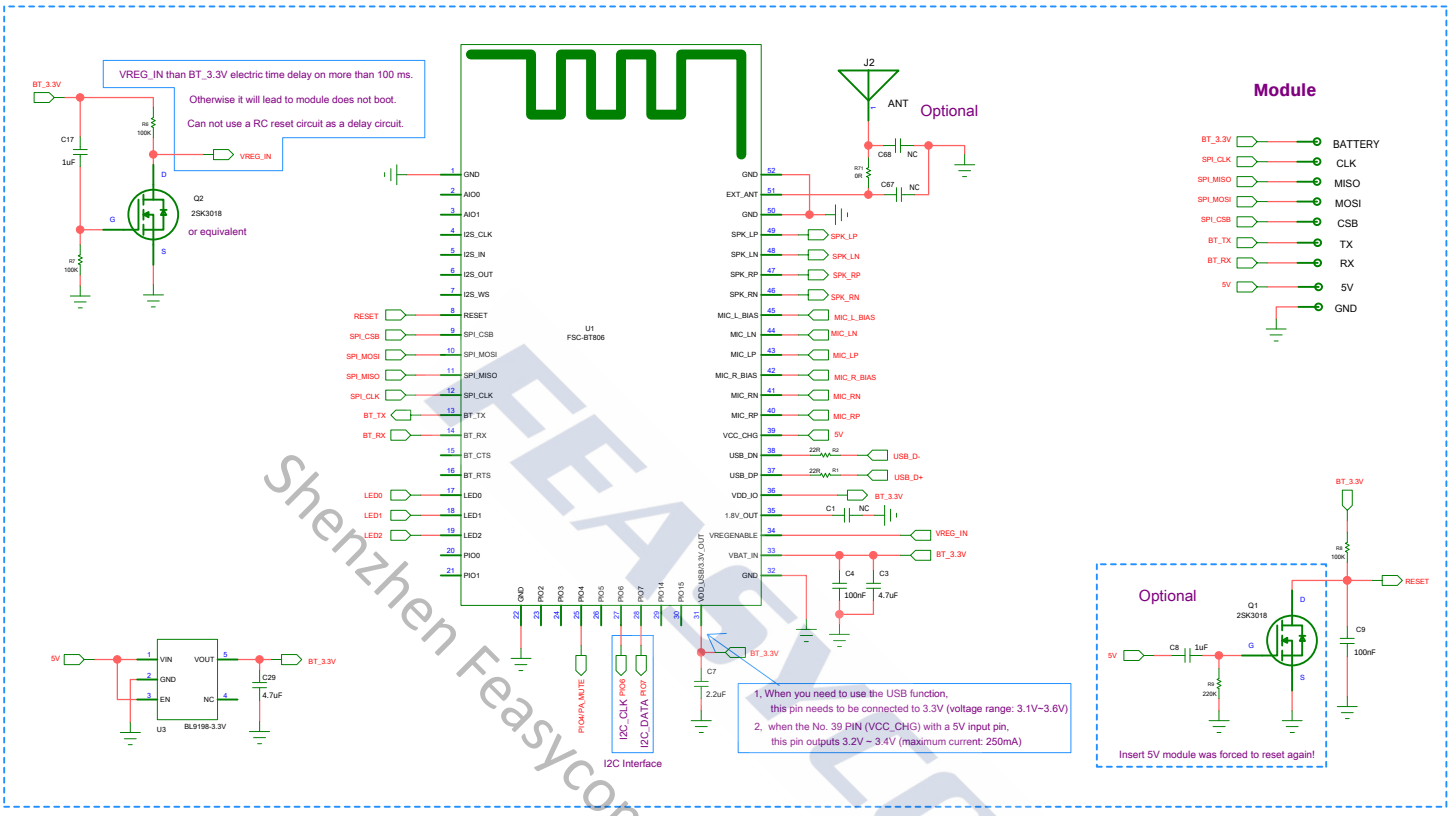
* If require any other packing, must be confirmed with customer

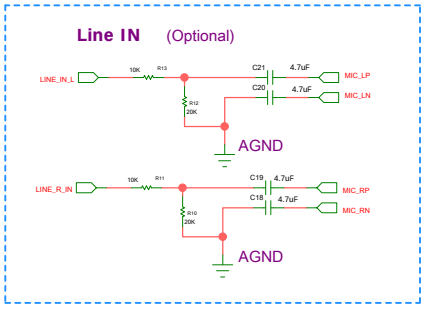
* Package: 2000PCS Per Carton (Min Carton Package)

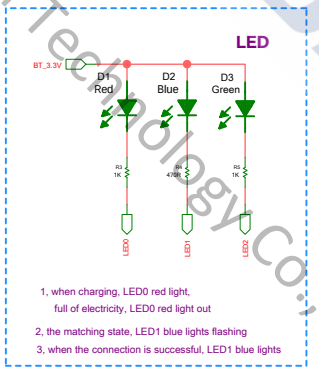
Figure 40: Packing Box

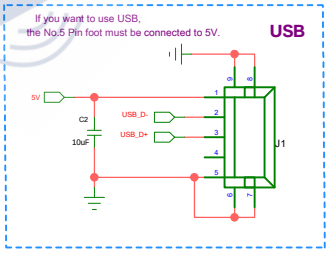
11. APPLICATION SCHEMATIC

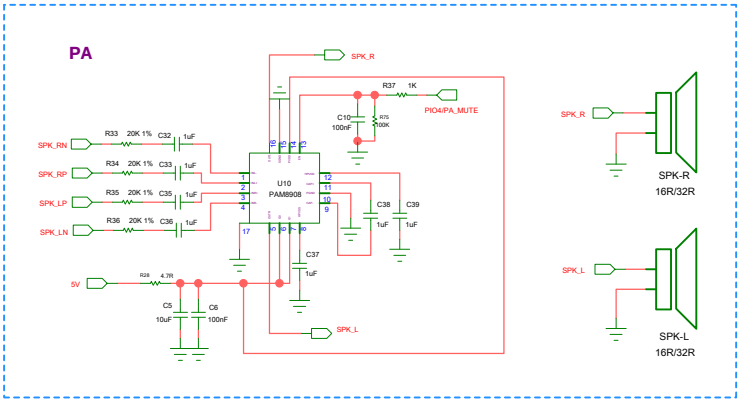
11.1 Application circuit diagram(Default)

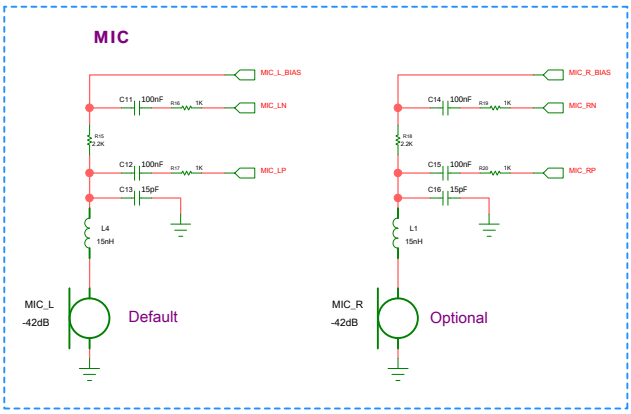












11.2 Application circuit diagram(Earphone)