32-bit Microcontrollers Addressing Automotive Audio System Control and CAN-MOST Gateway on 1 Chip FR Family **MB91F467M**

This product integrates MediaLB to connect seamlessly to multimedia automotive LAN specification MOST, audio interface I²S, standard automotive LAN specifications CAN, LIN, I²C, and many other peripheral resources. The "FR" CPU core, which is capable of fast control, enables this microcontroller to have system control of automotive audio on 1 chip.

* MOST: <u>M</u>edia-<u>O</u>riented <u>Systems</u> <u>T</u>ransport

* MediaLB: <u>Media L</u>ocal <u>B</u>us

Overview

MOST is a multimedia automotive LAN standard used by nearly all European automobile manufacturers including Audi, BMW, Land Rover, DaimlerChrysler, Porsche, Saab, and Volvo. It allows CD changers, radios, GPSs, cellular phones, and DVD players to be assigned in a ring network and deliver high-quality audio signals. As a standard specification to transmit data between MOST and IC, MediaLB was developed. MediaLB is a local serial bus that connects to the MOST network controller and operates in synchronization with MOST. Although I²C and I²S were previously the conventional methods used to connect to the MOST network controller, it is now possible to transmit streaming data, packet data, and control command data at high speed using MediaLB.

"MB91F467M" we have developed this time is capable of the simultaneous transmission of 10 stereo music sources to MediaLB. It also has a built-in CAN in addition to the 32-bit RISC CPU FR60 core, enabling a new solution linking the invehicle control network and the data network, "CAN-MOST gateway." Moreover, its built-in shutdown function leads to dramatic reduction in current consumption during standby.

Photo 1 External View



Product Features

Fig.1 presents the block diagram. This product's built-in resources deliver the following features:

FR60 core

This product adopts an FR60 core that is instruction-compatible with the FR series. This core is FUJITSU's 32-bit RISC CPU core that realizes high performance and low power consumption and is capable of operation at a maximum operation frequency of 80MHz.

Built-in Flash memory density

- Main Flash memory: 1,088Kbytes
- Flash memory security realized

Built-in RAM density

- 64Kbytes
- Direct mapped cache: 8Kbytes
- Instruction cache: 4Kbytes

Audio interface

• I²S interface: 10 channels

MediaLB controller

IP licensed and provided by SMSC. It is connected to I²S via the FIFO buffer and enables communication with MediaLB as the bus master (**Fig.2**). By using the circulation and

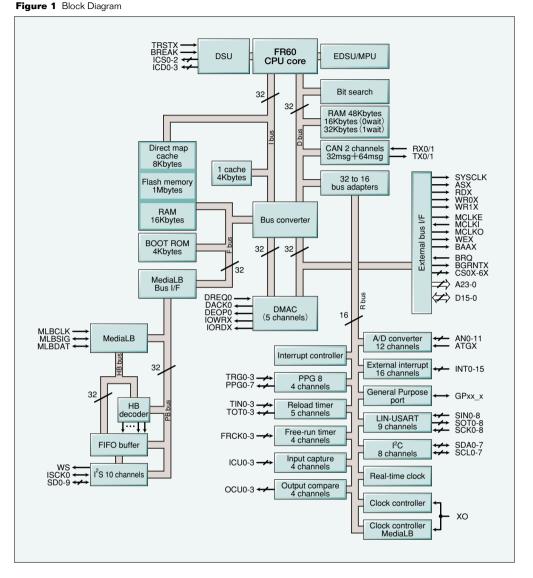
ping-pong buffering which is the DMA mode of MediaLB, streaming data is automatically transmitted between MediaLB- (FIFO buffer)- I²S.

CAN controller

Conforms to Parts A and B of CAN Specification Revision 2.0. There are 2 channels of 32 and 64 built-in message buffers for data and ID with ranking. Supports communication speed up to 1Mbps.

Various timers

- 16-bit free-run timer: 4 channels
- 16-bit input capture: 4 channels
- 16-bit output compare: 4 channels
- 16-bit PPG: 8 channels



16-bit reload timer: 5 channels

Various interfaces

- •LIN-supporting USART: 9 channels (4 channels with built-in FIFO)
- I²C interface: 8 channels
- External bus interface (address: 24-bit, data: 16-bit)

High-speed A/D converter

Sequential conversion A/D converter realizing 10-bit resolution: 16 channels (Minimum conversion time 3μ s, total error ± 3 LSB: Vcc=Avcc=3.0 to 3.6V)

Low power consumption mode: Sleep/stop/shutdown mode

The low power consumption modes are sleep mode (program

stops) and stop mode (device stops). It also integrates shutdown mode (power supply is cut). In shutdown mode, power supply is cut off for all parts except for RAM (64Kbytes) and shutdown control circuit and the standby current consumption (standard: $10 \,\mu$ A) can thus be reduced dramatically.

3V/5V terminals

Although the CPU power supply is 3V, the 3V/5V terminals are divided in 3 blocks and it is possible to set up terminals as 3V or 5V for each block.

I/O port

- Input permission setting: Setting possible for each port
- •Input level setting: Selection possible from 4 input levels: CMOS hysteresis (0307 or 0208)/Automotive (hysteresis)/TT
- Pull-up resistor setting: Setting possible for each port (standard: $50k\Omega$)

 Table 1 presents the selection of port input levels.

Other peripheral functions

- External interrupt: ×16 channels
- DMAC: ×5 channels
- •On-chip debugging support unit (DSU4)
- Real-time clock
- Watchdog timer
- Power supply voltage: 3.0 to 3.6V/3.0 to 5.5V
- Package: FPT-216P-M01 (LQFP-216-pin)

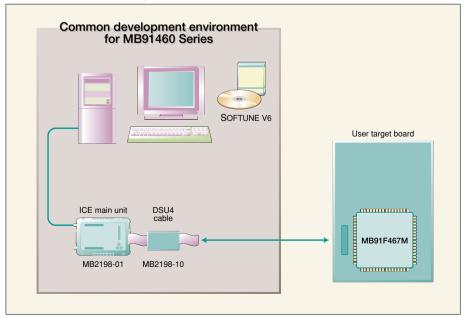
Figure 2 MediaLB/ I²S Connection Diagram

MediaLB MLBCLK H MLBDAT WS SD0-9 MLBCLK CPU MLBCLK CPU MLBCLK CPU MLBCLK CPU MLBCLK CPU

Table 1 Selection of Port Input Levels

Item	VIL (V)	VIH (V)	Input level
Input voltage	0.3Vcc	0.7Vcc	CMOS hysteresis
	0.2Vcc	0.8Vcc	CMOS hysteresis
	0.5Vcc	0.8Vcc	Automotive (hysteresis)
	0.8	2.1	TTL

Figure 3 Configuration of Development Tools



Development Environment

Like the conventional FR Series, this product is supported by the FUJITSU integrated development environment SOFTUNE V6. SOFTUNE V6 application software is designed to simplify programming tasks in order to satisfy the diverse needs of program designers. Since this product has a built-in debugging support unit, it allows debugging on the user board by integrating a special DSU connector on board.

Table 2 and Fig.3 present the development tools.

Evaluation Environment

FUJITSU plans to offer a MediaLB evaluation board and sample software as the development environment for beginning MediaLB using this product. MediaLB Evaluation board, MediaLB Low Level Driver, CAN, and I²S drivers will be available to support MediaLB development. We plan to offer the following tools: **Evaluation board**

MediaLB Evaluation board

Sample software

- Sample Application
- MediaLB Low Level Driver
- Net Services Ver. 2.x (binary provision)*
- * Please purchase the formal version from SMSC.

Fig.4 presents the evaluation environment configuration.

Application Fields

This product realizes in-vehicle rear audio entertainment in a simple manner. It is capable of the simultaneous transmission of up to 10 different streaming data and also simultaneously transmitting streaming data, packet data for web downloading and so forth, and command data for mechanical control. It also realizes a gateway between automotive control LANs such as CAN and LIN and MOST. Along with other peripheral functions, it is optimal for system control of audio center units.

Fig.5 presents an example block diagram of a car audio system adopting this product. **Fig.6** presents an example of a new solution linking the in-vehicle control network and data network "MOST-CAN gateway."

Table 2 Development Tools

Hardware	Emulator main unit	MB2198-01	
	DSU4 cable	MB2198-10	
	Chip	MB91F467M	
Software	SOFTUNE V6 Workbench		
	SOFTUNE V6 C compiler		
	SOFTUNE V6 assembler		
	SOFTUNE V6 C/C++ analyzer		
	SOFTUNE V6 C checker		

Figure 4 Evaluation Environment Configuration

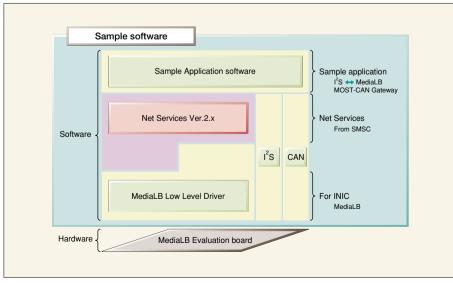


Figure 5 System Block Diagram for Automotive Audio System Using MB91F467M

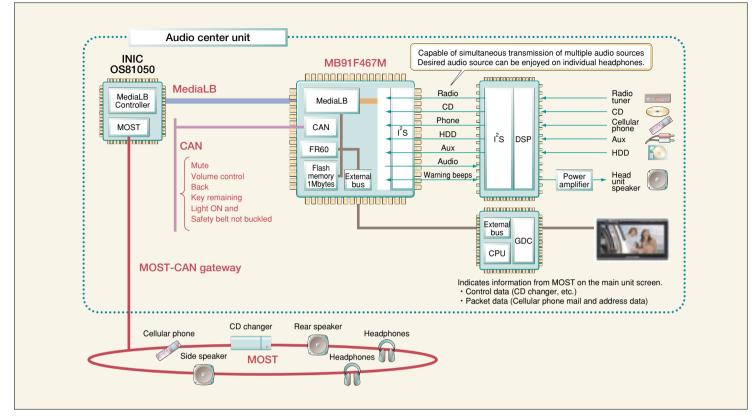


Figure 6 Example of Coordination between Control System Network and Information System Network: CAN-MOST Gateway

