



# PCM1801

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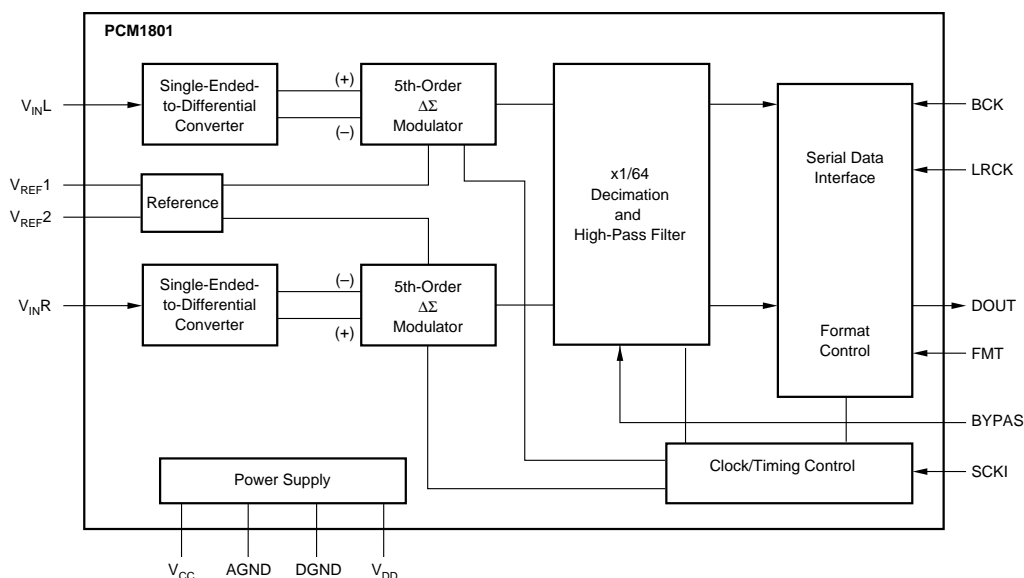
## 16-Bit, Stereo, Audio ANALOG-TO-DIGITAL CONVERTER

### FEATURES

- DUAL 16-BIT MONOLITHIC  $\Delta\Sigma$  ADC
- SINGLE-ENDED VOLTAGE INPUT
- 64X OVERSAMPLING DECIMATION FILTER:  
Passband Ripple:  $\pm 0.05\text{dB}$   
Stopband Attenuation:  $-65\text{dB}$
- ANALOG PERFORMANCE:  
THD+N:  $-88\text{dB}$  (typ)  
SNR:  $93\text{dB}$  (typ)  
Dynamic Range:  $93\text{dB}$  (typ)  
Internal High-Pass Filter
- PCM AUDIO INTERFACE: Left Justified, I<sup>2</sup>S
- SAMPLING RATE:  $4\text{kHz}$  to  $48\text{kHz}$
- SYSTEM CLOCK:  $256f_s$ ,  $384f_s$ , or  $512f_s$
- SINGLE  $+5\text{V}$  POWER SUPPLY
- SMALL SO-14 PACKAGE

### DESCRIPTION

PCM1801 is a low cost, single chip stereo analog-to-digital converter with single-ended analog voltage inputs. The PCM1801 uses a delta-sigma modulator with 64x oversampling, a digital decimation filter, and a serial interface which supports Slave mode operation and two data formats. The PCM1801 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required.



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Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

All specifications at +25°C, +V<sub>DD</sub> = +V<sub>CC</sub> = +5V, f<sub>S</sub> = 44.1kHz, and 16-bit data, SYSCLK = 384f<sub>S</sub>, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1801U			UNITS
		MIN	TYP	MAX	
<b>RESOLUTION</b>		16			Bits
<b>DIGITAL INPUT/OUTPUT</b>					
Input Logic Level:					
V <sub>IH</sub> <sup>(1)</sup>		2.0			V
V <sub>IL</sub> <sup>(1)</sup>				0.8	V
Input Logic Current:					
I <sub>IN</sub> <sup>(2)</sup>				±1	μA
I <sub>IN</sub> <sup>(3)</sup>				+100	μA
Output Logic Level:					
V <sub>OH</sub> <sup>(4)</sup>	I <sub>OH</sub> = -1.6mA	4.5			V
V <sub>OL</sub> <sup>(4)</sup>	I <sub>OL</sub> = +3.2mA			0.5	V
Sampling Frequency		4	44.1	48	kHz
System Clock Frequency	256f <sub>S</sub>	1.024	11.2896	12.2880	MHz
	384f <sub>S</sub>	1.536	16.9344	18.4320	MHz
	512f <sub>S</sub>	2.024	22.5792	24.5760	MHz
<b>DC ACCURACY</b>					
Gain Mismatch Channel-to-Channel			±1.0	±2.5	% of FSR
Gain Error			±2.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error	High-Pass Filter Bypass		±2.0		% of FSR
Bipolar Zero Drift	High-Pass Filter Bypass		±20		ppm of FSR/°C
<b>DYNAMIC PERFORMANCE<sup>(5)</sup></b>					
THD+N at FS (-0.5dB)			-88	-80	dB
THD+N at -60dB			-90		dB
Dynamic Range	EIAJ, A-weighted	90	93		dB
Signal-To-Noise Ratio	EIAJ, A-weighted	90	93		dB
Channel Separation		88	91		dB
<b>ANALOG INPUT</b>					
Input Range	FS (V <sub>IN</sub> = 0dB)		2.828		Vp-p
Center Voltage			2.1		V
Input Impedance			30		kΩ
Anti-Aliasing Filter Frequency Response	-3dB		170		kHz
<b>DIGITAL FILTER PERFORMANCE</b>					
Passband				0.454f <sub>S</sub>	Hz
Stopband		0.583f <sub>S</sub>			Hz
Passband Ripple				±0.05	dB
Stopband Attenuation		-65			dB
Delay Time (Latency)			17.4/f <sub>S</sub>		sec
High Pass Frequency Response	-3dB			0.019f <sub>S</sub>	mHz
<b>POWER SUPPLY REQUIREMENTS</b>					
Voltage Range	+V <sub>CC</sub>	+4.5	+5.0	+5.5	VDC
	+V <sub>DD</sub>	+4.5	+5.0	+5.5	VDC
Supply Current <sup>(6)</sup>	+V <sub>CC</sub> = +V <sub>DD</sub> = +5V		18	25	mA
Power Dissipation	+V <sub>CC</sub> = +V <sub>DD</sub> = +5V		90	125	mW
<b>TEMPERATURE RANGE</b>					
Operation		-25		+85	°C
Storage		-55		+125	°C
Thermal Resistance, θ <sub>JA</sub>			100		°C/W

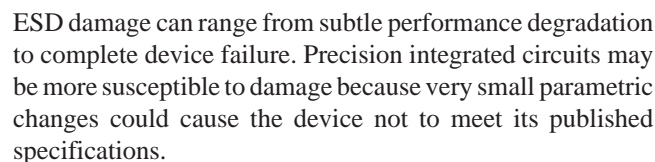
NOTES: (1) Pins 5, 6, 7, 9, and 10 (SCKI, BCK, LRCK, BYPAS, FMT). (2) Pins 5, 6, 7 (SCKI, BCK, LRCK) Schmitt-Trigger input. (3) Pins 9, 10 (BYPAS, FMT) Schmitt-Trigger input with 100kΩ typical pull-down resistor. (4) Pin 8 (DOUT). (5) f<sub>IN</sub> = 1kHz, using Audio Precision's System II, rms Mode with 20kHz LPF and 400Hz HPF enabled. (6) No load on DOUT (pin 8).

**Top View** **SOIC**

Pin	Signal	Signal	Pin
1	$V_{INL}$	$V_{REF1}$	14
2	$V_{INR}$	$V_{REF2}$	13
3	DGND	AGND	12
4	$V_{DD}$	$V_{CC}$	11
5	SCKI	FMT	10
6	BCK	BYPAS	9
7	LRCK	DOUT	8

PIN	NAME	I/O	DESCRIPTION
1	V <sub>IN</sub> L	IN	Analog Input, Lch.
2	V <sub>IN</sub> R	IN	Analog Input, Rch.
3	DGND	—	Digital Ground
4	V <sub>DD</sub>	—	Digital Power Supply
5	SCKI	IN	System Clock Input; 256f <sub>S</sub> , 384f <sub>S</sub> , or 512f <sub>S</sub> .
6	BCK	IN	Bit Clock Input
7	LRCK	IN	Sampling Clock Input
8	DOUT	OUT	Audio Data Output
9	BYPAS	IN	HPF Bypass Control <sup>(1)</sup> L: HPF Enabled H: HPF Disabled
10	FMT	IN	Audio Data Format <sup>(1)</sup> L: MSB-First, Left-Justified H: MSB-First, I <sup>2</sup> S
11	V <sub>CC</sub>	—	Analog Power Supply
12	AGND	—	Analog Ground
13	V <sub>REF</sub> 2	—	Reference 2 Decoupling Capacitor
14	V <sub>REF</sub> 1	—	Reference 1 Decoupling Capacitor

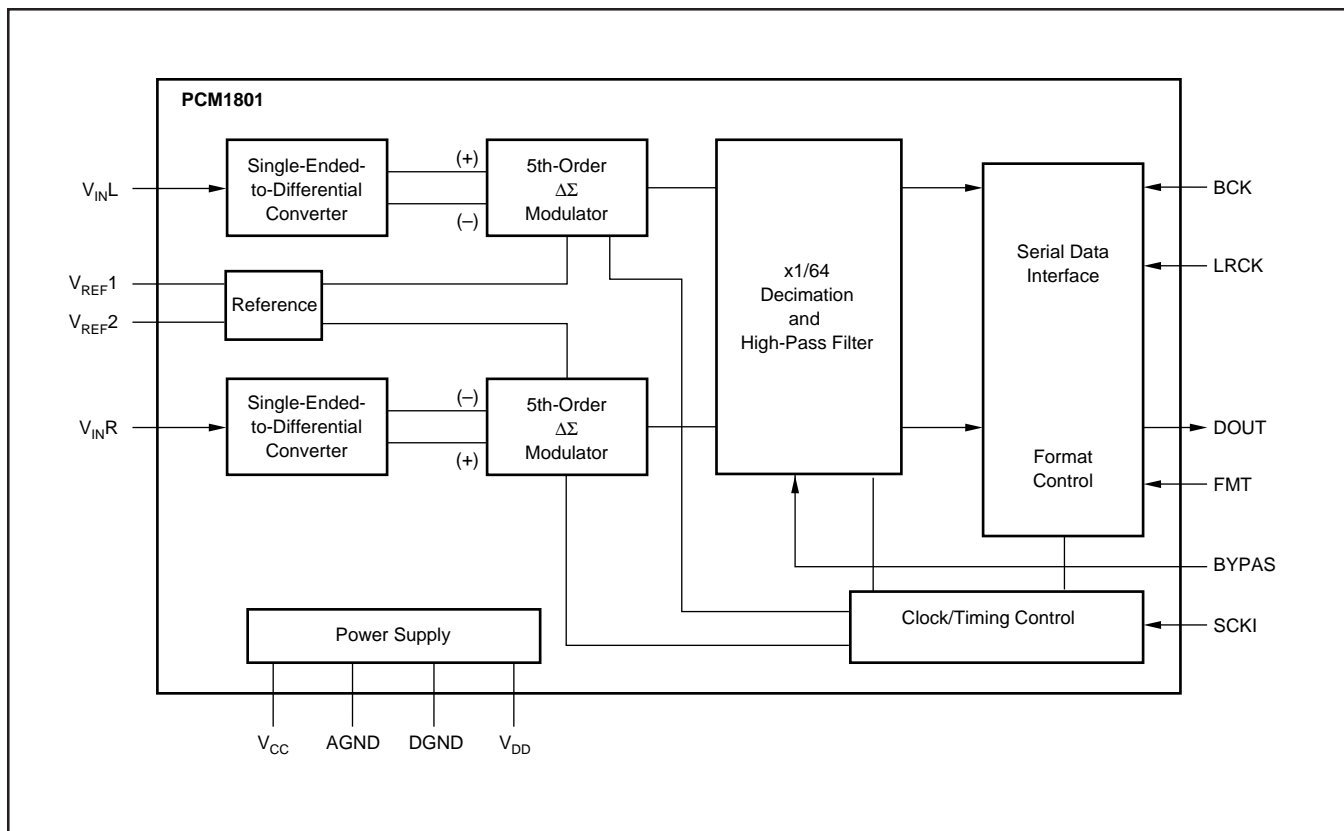
Supply Voltage: +V <sub>DD</sub> , +V <sub>CC</sub>	+6.5V
Supply Voltage Differences	±0.1V
GND Voltage Differences	±0.1V
Digital Input Voltage	-0.3V to (V <sub>DD</sub> + 0.3V)
Analog Input Voltage	-0.3V to (V <sub>CC</sub> + 0.3V)
Input Current (any pin except supplies)	±10mA
Power Dissipation	300mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature	-55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
(reflow, 10s)	+235°C



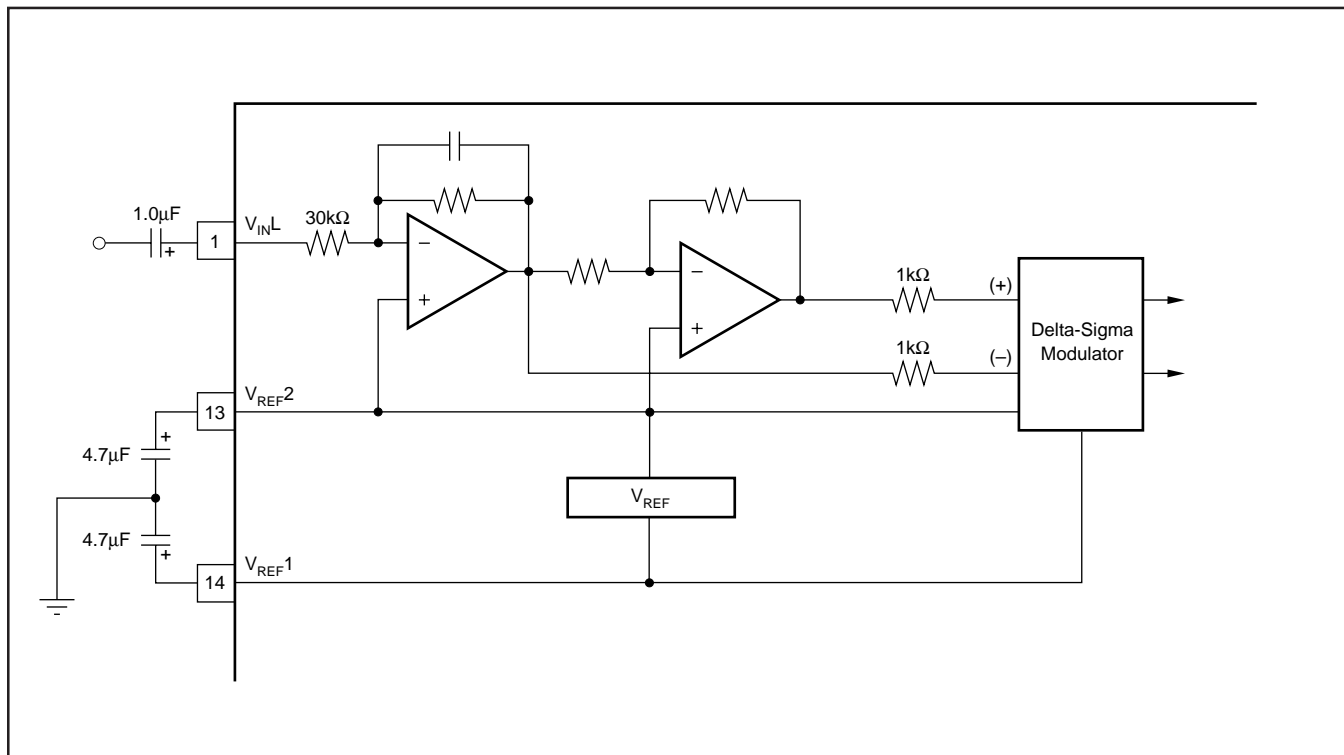
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(1)</sup>	TRANSPORT MEDIA
PCM1801U "	SO-14 "	235 "	-25°C to +85°C "	PCM1801U "	PCM1801U PCM1801U/2K	Rails Tape and Reel

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## BLOCK DIAGRAM



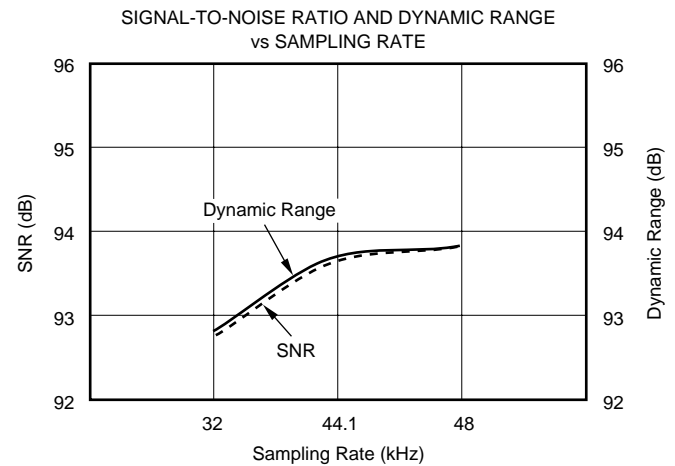
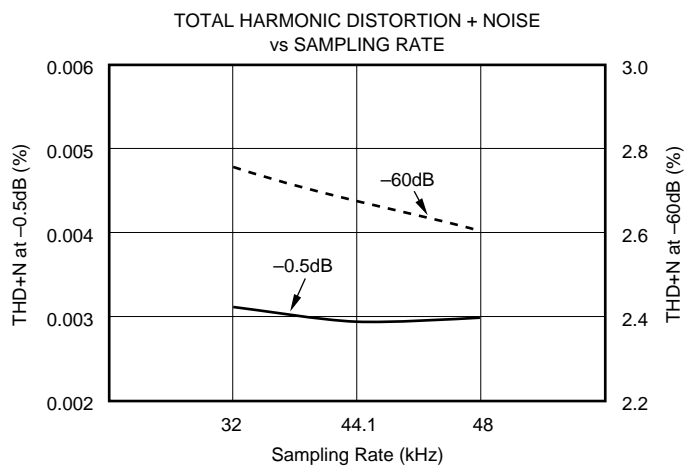
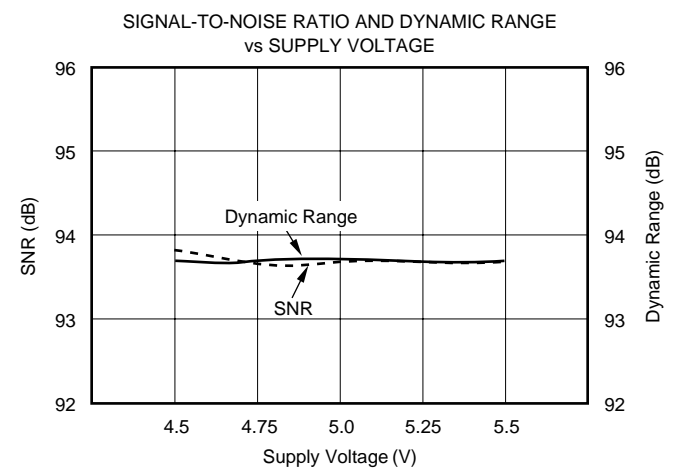
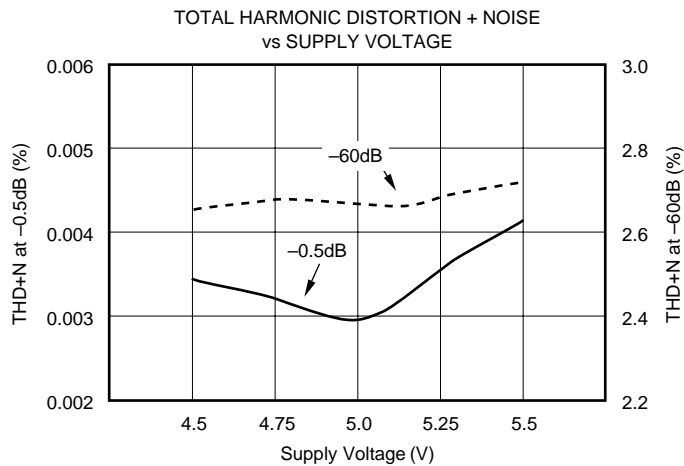
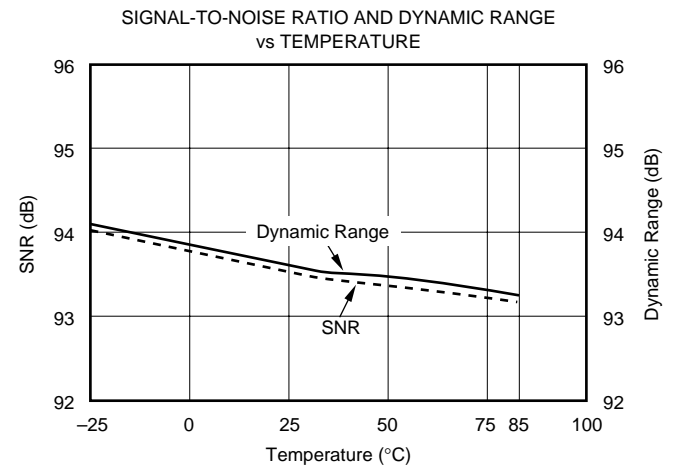
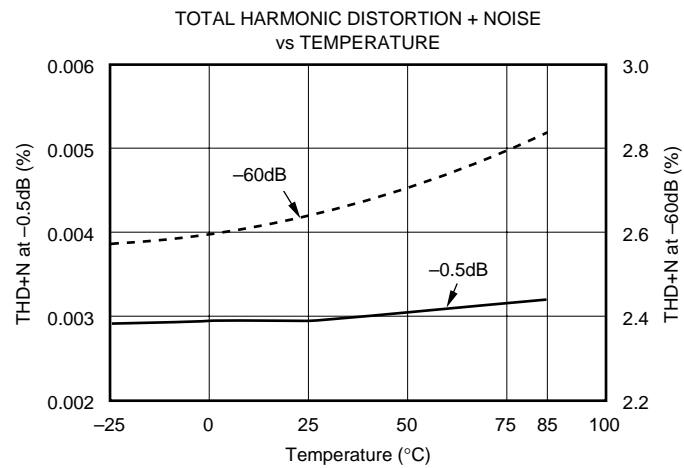
## ANALOG FRONT-END (Single-Channel)



# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +V_{CC} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , and  $\text{SYSCLK} = 384f_S$ , unless otherwise noted.

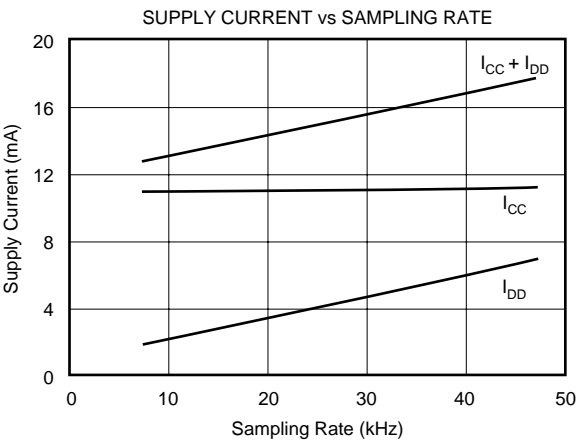
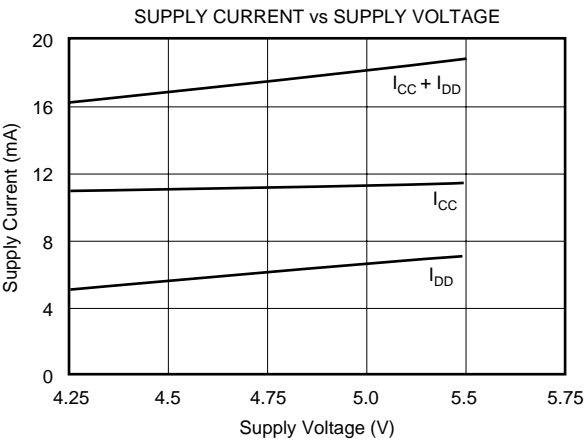
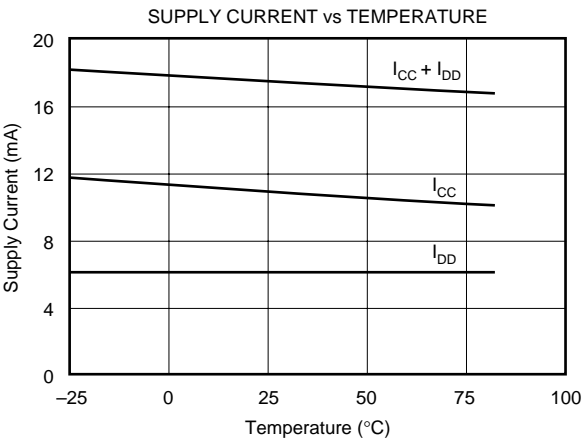
## ANALOG DYNAMIC PERFORMANCE



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^{\circ}\text{C}$ ,  $+V_{DD} = +V_{CC} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , and  $\text{SYSCLK} = 384f_S$ , unless otherwise noted.

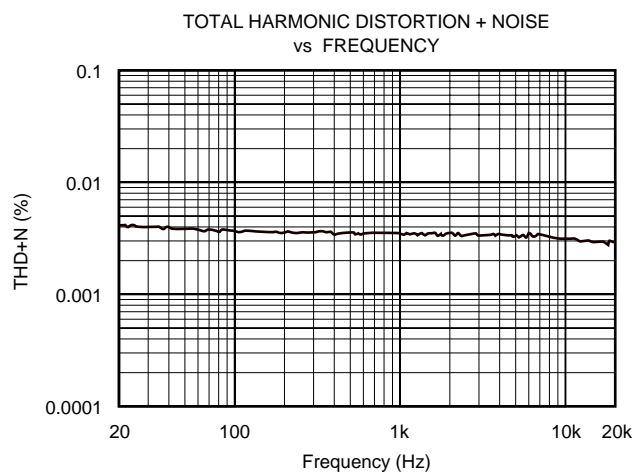
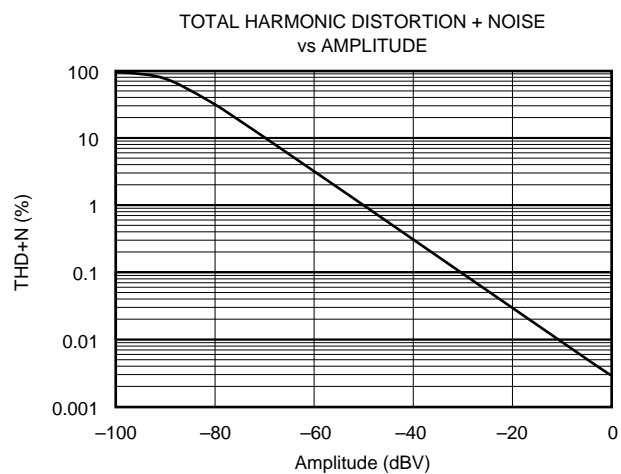
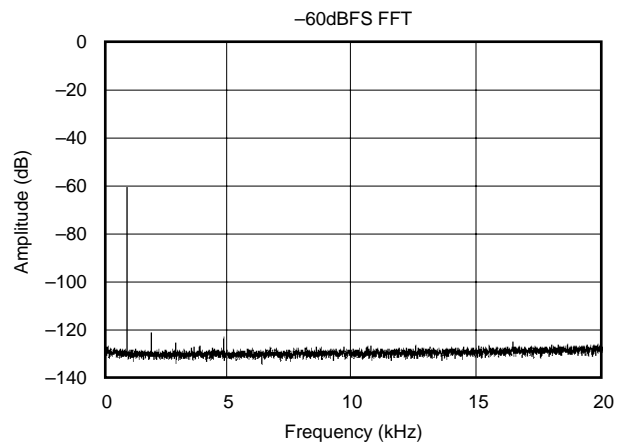
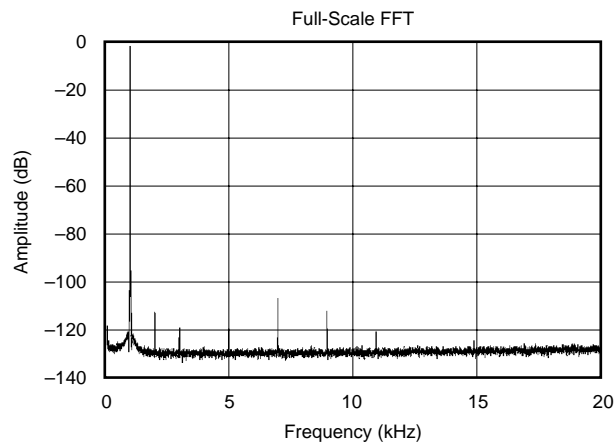
## ANALOG DYNAMIC PERFORMANCE (cont.)



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +V_{CC} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , and  $\text{SYSCLK} = 384f_S$ , unless otherwise noted.

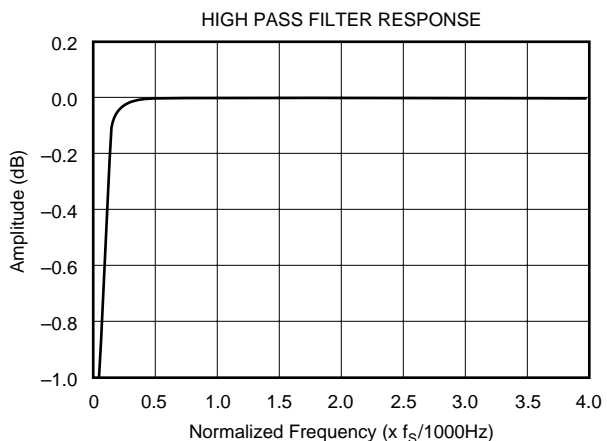
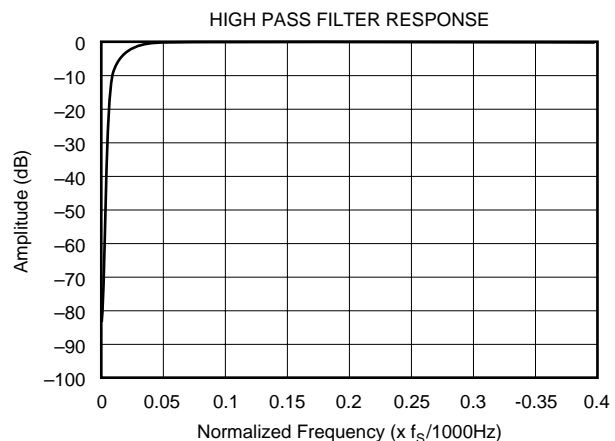
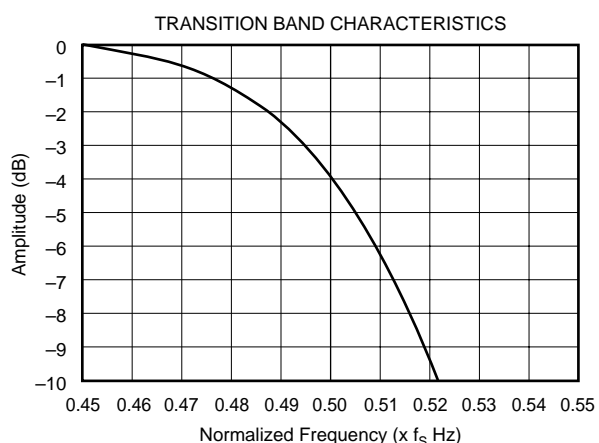
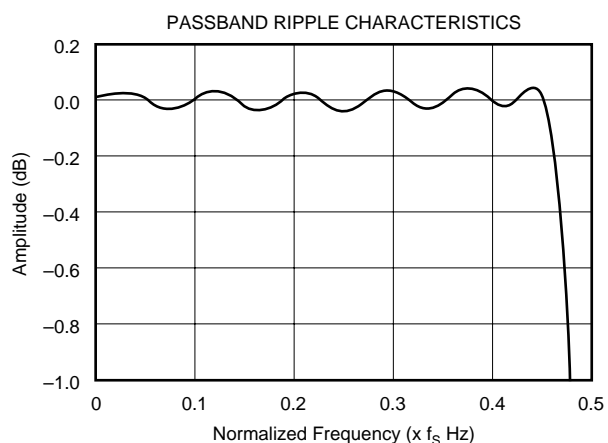
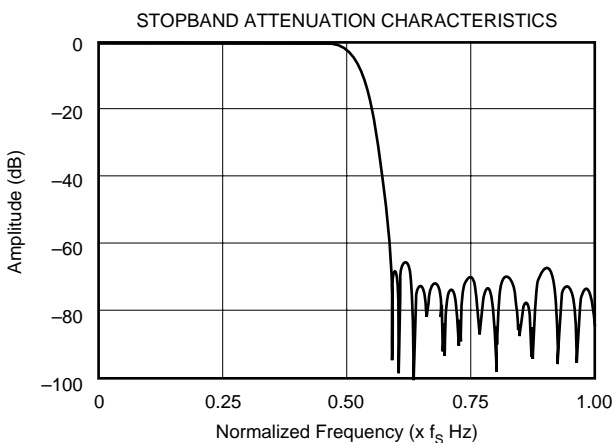
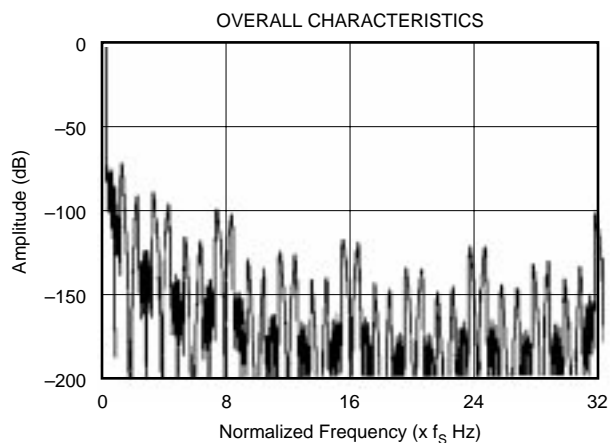
## OUTPUT SPECTRUM



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +V_{CC} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , and  $\text{SYSCLK} = 384f_S$ , unless otherwise noted.

## DIGITAL FILTER

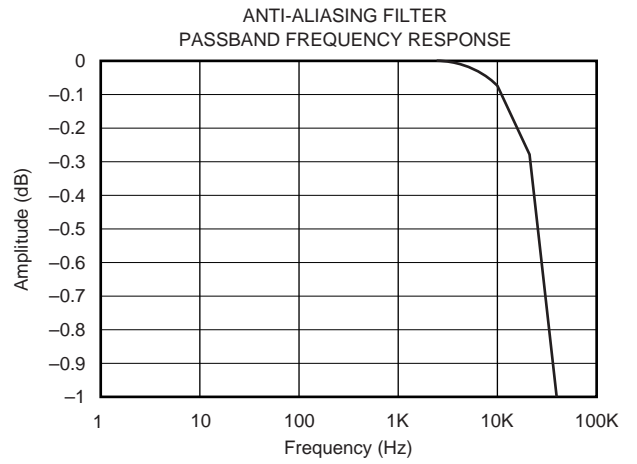
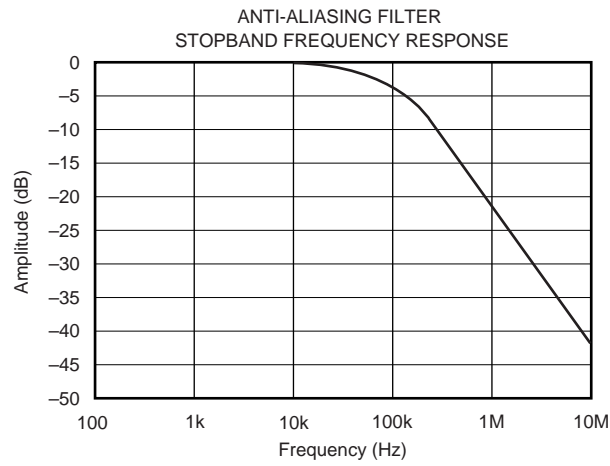




# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +V_{CC} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , and  $\text{SYSCLK} = 384f_S$ , unless otherwise noted.

## ANTI-ALIASING



# THEORY OF OPERATION

PCM1801 consists of a bandgap reference, two channels of a single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The Block Diagram illustrates the total architecture of PCM1801, the Analog Front-End diagram illustrates the architecture of the single-to-differential converter, and the anti-aliasing filter is illustrated in the Block Diagram. Figure 1 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal high precision reference with two external capacitors provides all reference voltages which are required by the converter, and defines the full-scale voltage range of both channels. The internal single-ended to differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full differential architecture provides a wide dynamic range and excellent power supply rejection performance.

The input signal is sampled at 64x oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator and a feedback loop consisting of a 1-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The  $64f_s$ , 1-bit stream from the modulator is converted to  $1f_s$ , 16-bit digital data by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The DC components are removed by a digital high-pass filter, and the filtered output is converted to time-multiplexed serial signals through a serial interface which provides flexible serial formats.

## SYSTEM CLOCK

The system clock for PCM1801 must be either  $256f_s$ ,  $384f_s$ , or  $512f_s$ , where  $f_s$  is the audio sampling frequency. The system clock must be supplied on SCKI (pin 5).

PCM1801 also has a system clock detection circuit which automatically senses if the system clock is operating at  $256f_s$ ,  $384f_s$ , or  $512f_s$ .

When  $384f_s$  and  $512f_s$  system clock are used, the PCM1801 automatically divides these clocks down to  $256f_s$  internally. This  $256f_s$  clock is used to operate the digital filter and the modulator. Table I lists the relationship of typical sampling frequencies and system clock frequencies. Figure 2 illustrates the system clock timing.

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	256f <sub>s</sub>	384f <sub>s</sub>	512f <sub>s</sub>
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48	12.2880	18.4320	24.5760

TABLE I. System Clock Frequencies.

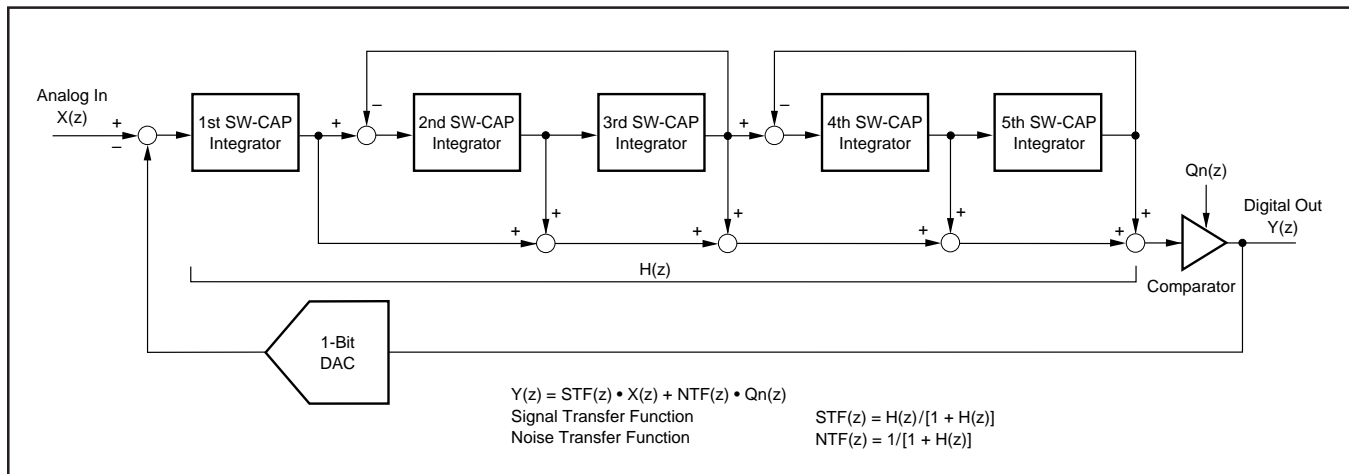


FIGURE 1. Simplified Diagram of the PCM1801 5th-Order Delta-Sigma Modulator.

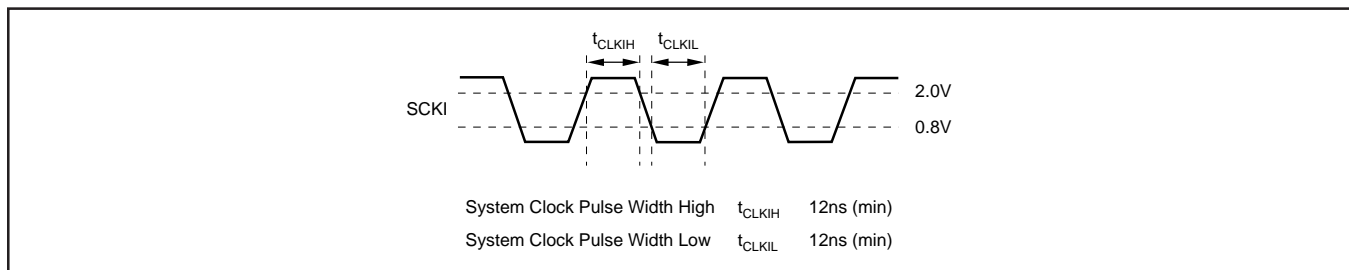


FIGURE 2. System Clock Timing.

## RESET

PCM1801 has an internal power-on reset circuit, which initializes (resets) when the supply voltage ( $V_{CC}/V_{DD}$ ) exceeds 4.0V (typ). The PCM1801 stays in the reset state and the digital output is forced to zero. The digital output is valid after reset state release and 18436f<sub>s</sub> periods. During reset, the logic circuits and the digital filter stop operating. Figure 3 illustrates the internal power-on reset timing.

## SERIAL AUDIO DATA INTERFACE

The PCM1801 interfaces the audio system through BCK (pin 6), LRCK (pin 7), and DOUT (pin 8).

### DATA FORMAT

PCM1801 supports two audio data formats in Slave Mode, and are selected by the FMT control input (pin 10) as shown in Table II.

FMT	DATA FORMAT
0 (L)	16-Bit, Left-Justified
1 (H)	16-Bit, I <sup>2</sup> S

TABLE II. Data Format.

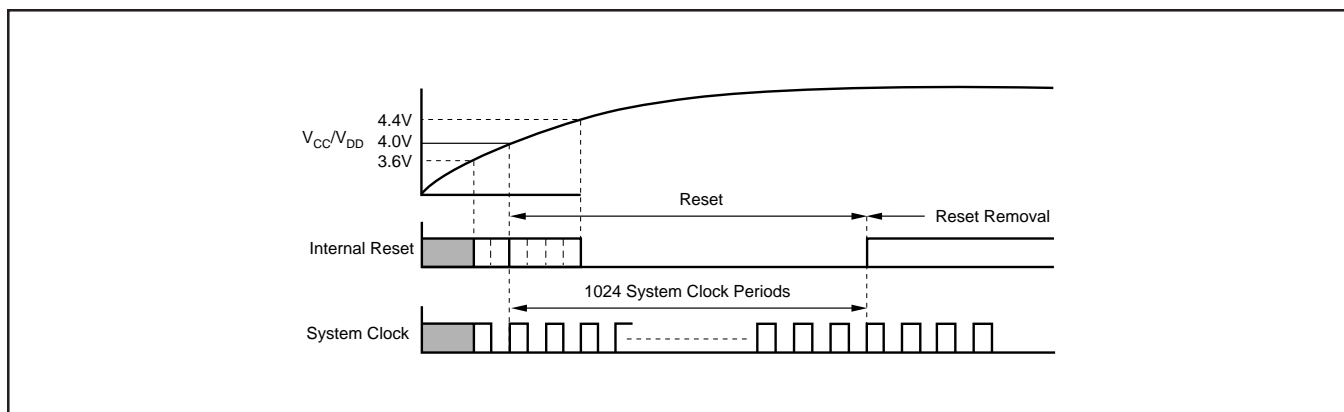


FIGURE 3. Internal Power-On Reset Timing.

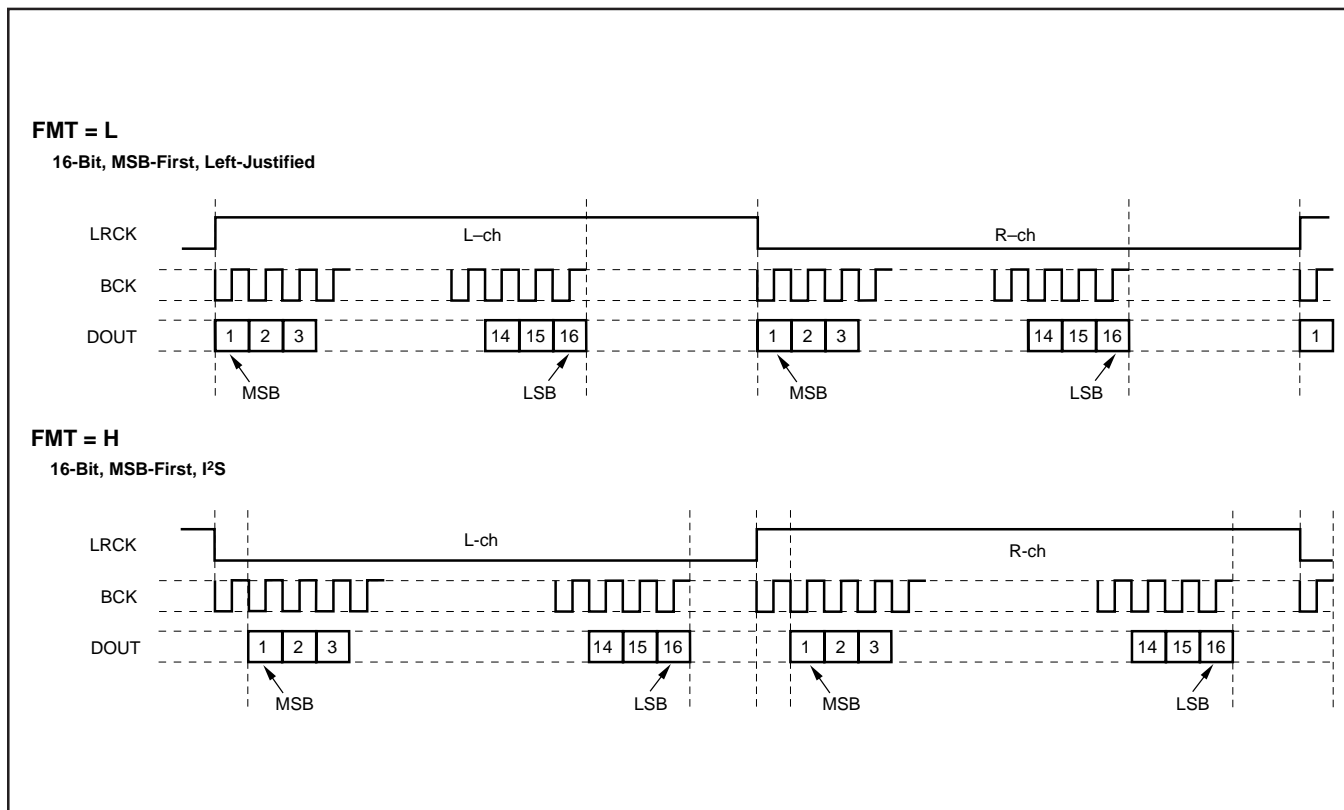


FIGURE 4. Audio Data Format (Slave Mode: LRCK, and BCK are inputs).

# SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

PCM1801 operates with LRCK synchronized to the system clock (SCKI). PCM1801 does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI. If the relationship between LRCK and SCKI changes more than 6 bit clocks (BCK) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within  $1/f_s$  and the digital output is forced to BPZ until resynchronization between LRCK and SCKI is completed. In case of changes less than 5 bit clocks (BCK), resynchronization does not occur and above digital output control and discontinuity does not occur.

## ADC DATA OUTPUT AT RESET

Figures 6 and 7 illustrate the ADC digital output for the reset operation and loss of synchronization state. During undefined data, it may generate some noise in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal makes a discontinuity of data on the digital output, and may generate some noise in the audio signal.

# BOARD DESIGN AND LAYOUT CONSIDERATIONS

## V<sub>CC</sub>, V<sub>DD</sub> PINS

The digital and analog power supply lines to the PCM1801 should be bypassed to the corresponding ground pins with both 0.1μF and 10μF capacitors as close to the pins as possible to maximize the dynamic performance of the ADC. Although PCM1801 has two power lines to maximize the potential of dynamic performance, using one common power supply is

recommended to avoid unexpected power supply problems, such as latch-up due to power supply sequencing.

## AGND, DGND PINS

To maximize the dynamic performance of the PCM1801, the analog and digital grounds are not internally connected. These points should have very low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the PCM1801 package to reduce potential noise problems.

## V<sub>IN</sub> PINS

A 1.0μF tantalum capacitor is recommended as an AC-coupling capacitor which establishes a 5.3Hz cut-off frequency. If a higher full-scale input voltage is required, the input voltage range can be increased by adding a series resistor to the V<sub>IN</sub> pins.

## V<sub>REF</sub> INPUTS

A 4.7μF tantalum capacitor is recommended between ground and the V<sub>REF1</sub> and V<sub>REF2</sub> references to ensure low source impedance. These capacitors should be located as close as possible to the V<sub>REF1</sub> or V<sub>REF2</sub> pins to reduce dynamic errors on the ADC's references.

## SYSTEM CLOCK

The quality of the system clock can influence dynamic performance in the PCM1801. The duty cycle, jitter, and threshold voltage at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCK), and word clock (LRCK) should also be supplied simultaneously. Failure to supply the audio clocks will result in a power dissipation increase of up to three times normal dissipation and may degrade long-term reliability if the maximum power dissipation limit is exceeded.

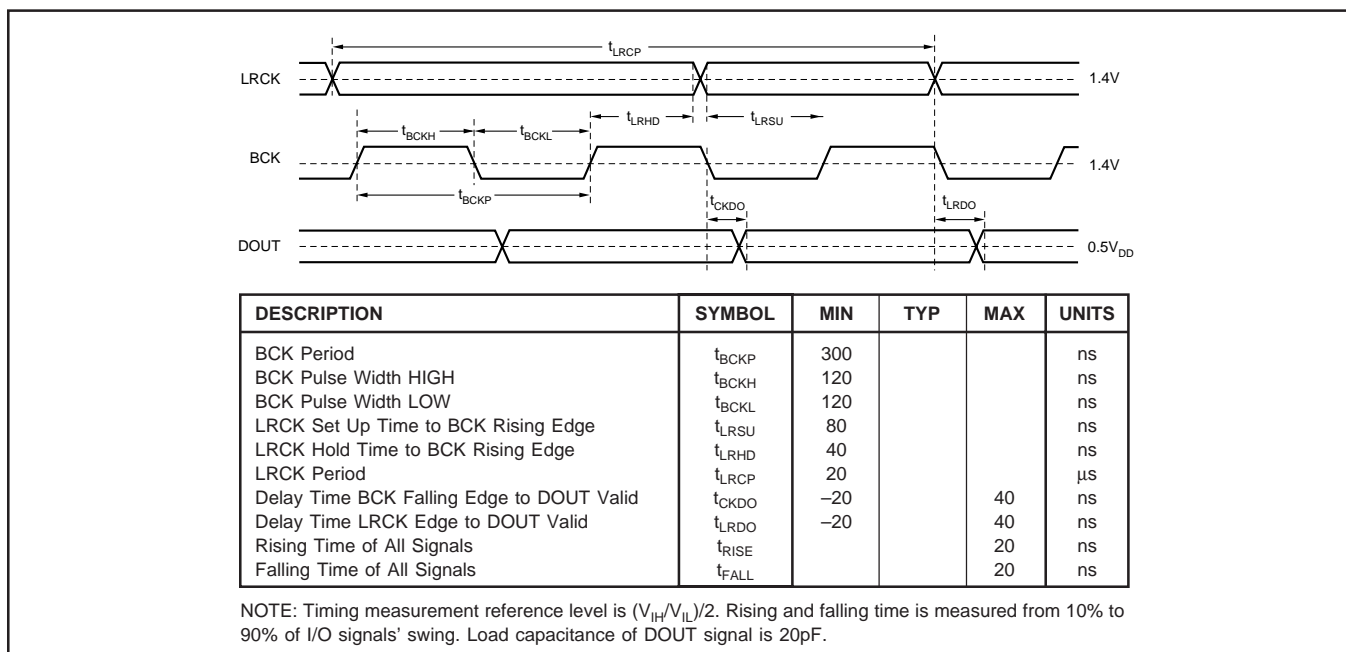


FIGURE 5. Audio Data Interface Timing (LRCK and BCK are inputs).

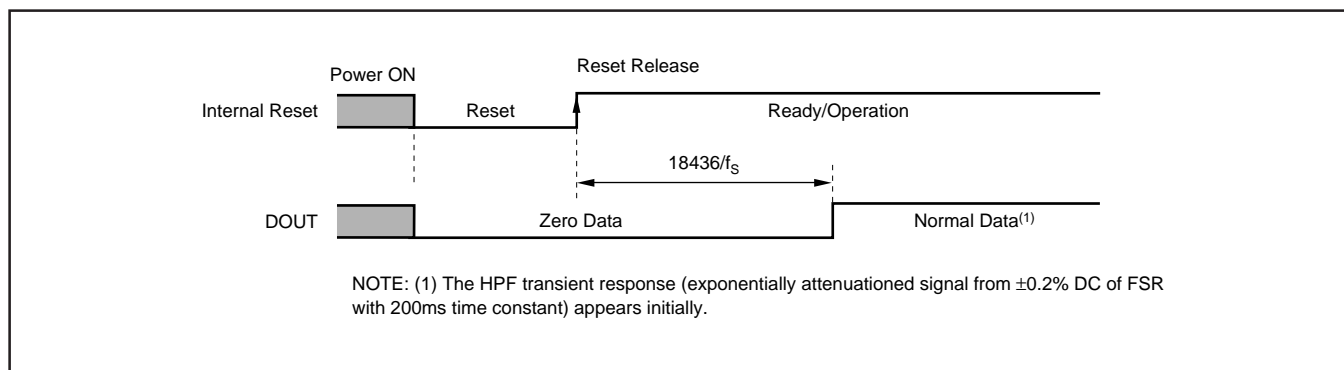


FIGURE 6. ADC Output for Power-On Reset and RSTB Control.

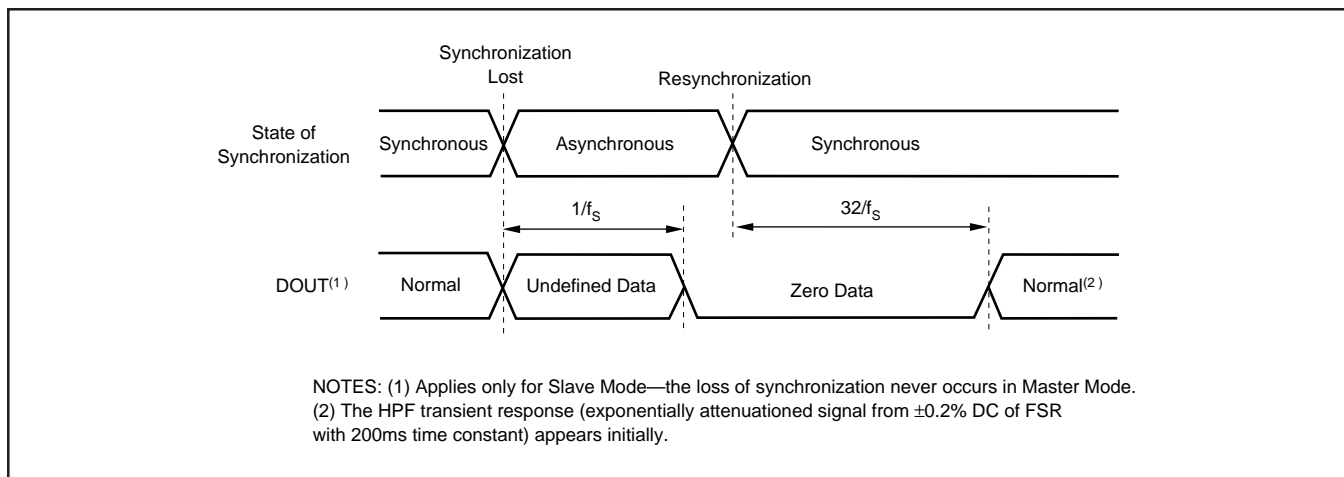


FIGURE 7. ADC Output for Loss of Synchronization.

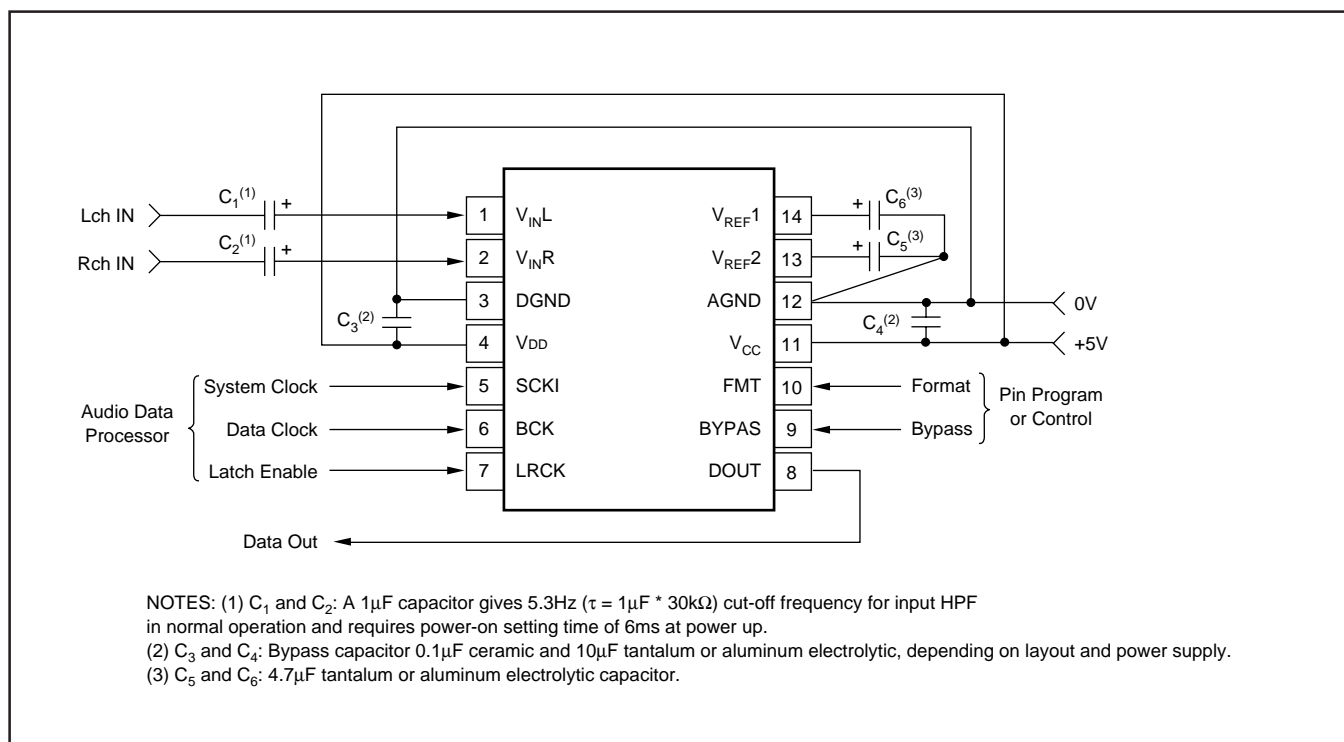


FIGURE 8. Typical Circuit Connection.

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