TRIPATH

TA2020-020

STEREO 20W (4Ω) CLASS-T™ DIGITAL AUDIO AMPLIFIER DRIVER USING DIGITAL POWER PROCESSING (DPP™) TECHNOLOGY

Technical Information **Revision 6.1 – April 2003**

GENERAL DESCRIPTION

The TA2020-020 is a 20W (4Ω) continuous average per channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing (DPP™) technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

APPLICATIONS

- DVD Players
- Mini/Micro Component Systems
- Computer / PC Multimedia
- Cable Set-Top Products
- Televisions
- Battery Powered Systems

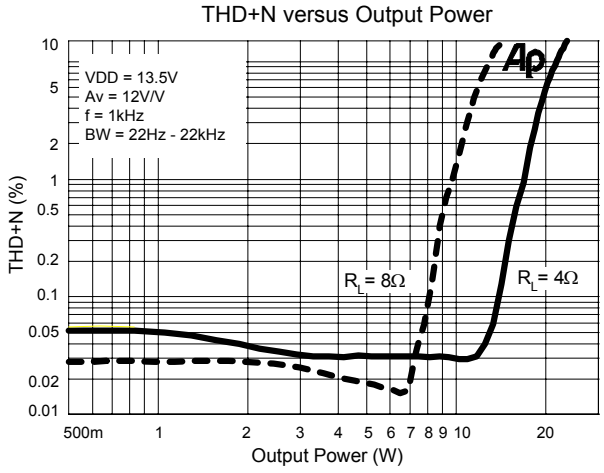
BENEFITS

- Fully integrated solution with internal FETs
- Easier to design-in than Class-D
- Reduced system cost with minimal heat sink requirement
- Dramatically improves efficiency versus Class-AB amplifiers
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD and DVD, and internet audio

FEATURES

- Class-T architecture
- Single Supply Operation
- "Audiophile" Quality Sound
  - 0.03% THD+N @ 10W 4Ω
  - 0.1% THD+N @12W 4Ω
  - 0.18% IHF-IM @ 1W 4Ω
- High Power
  - 25W @ 4Ω, 10% THD+N, V_{DD}=14.6V
  - 22W @ 4Ω, 10% THD+N, V_{DD}=13.5V
  - 13W @ 8Ω, 10% THD+N, V_{DD}=13.5V
- High Efficiency
  - 88% @ 12W 8Ω
  - 81% @ 20W 4Ω
- Dynamic Range = 99dB
- Mute and Sleep inputs
- Turn-on & turn-off pop suppression
- Over-current protection
- Over-temperature protection
- Bridged outputs
- 32-pin SSIP package

TYPICAL PERFORMANCE



ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	PARAMETER		Value	UNITS
V_{DD}	Supply Voltage		16	V
V5	Input Section Supply Voltage		6.0	V
SLEEP	SLEEP Input Voltage		-0.3 to 6.0	V
MUTE	MUTE Input Voltage		-0.3 to V5+0.3	V
ESD_{HBM}	ESD Susceptibility, Human Body Model (Note2)	All pins except 2, 30 Pins 2, 30	2000 1000	V V
ESD_{MM}	ESD Susceptibility, Machine Model (Note 3)		200	V
T_{STORE}	Storage Temperature Range		-40 to 150	°C
T_A	Operating Free-air Temperature Range		-40 to 85	°C
T_J	Junction Temperature		150	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. See the table below for Operating Conditions.
Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.
Note 3: Machine model, 220pF discharged through all pins.

OPERATING CONDITIONS (Note 4)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD}	Supply Voltage	8.5	13.5	14.6	V
V_{IH}	High-level Input Voltage (MUTE, SLEEP)	3.5			V
V_{IL}	Low-level Input Voltage (MUTE, SLEEP)			1	V

Note 4: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNITS
θ_{JC}	Junction-to-case Thermal Resistance	3.5°	C/W
θ_{JA}	Junction-to-ambient Thermal Resistance	15°	C/W

ELECTRICAL CHARACTERISTICS (Notes 6, 7)

See Test/Application Circuit. Unless otherwise specified, V_{DD} = 13.5V, f = 1kHz, Measurement Bandwidth = 22kHz, R_L = 4Ω, T_A = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_O	Output Power (Continuous Average/Channel)	THD+N = 0.1% R_L = 4Ω		11		W
		R_L = 8Ω		7		W
		THD+N = 10% R_L = 4Ω		18		W
		R_L = 8Ω		10		W
P_O	Output Power (V_{DD}=14.6V) (Continuous Average/Channel)	THD+N = 0.1% R_L = 4Ω		16.5		W
		R_L = 8Ω		9.5		W
		THD+N = 10% R_L = 4Ω		25		W
		R_L = 8Ω		14.8		W
$I_{DD,MUTE}$	Mute Supply Current	MUTE = V_{IH}		5.5	7	mA
$I_{DD, SLEEP}$	Sleep Supply Current	SLEEP = V_{IH}		0.25	2	mA
I_q	Quiescent Current	V_{IN} = 0 V		64	75	mA
THD + N	Total Harmonic Distortion Plus Noise	P_O = 10W/Channel		0.03		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF)		0.1	0.5	%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 20W, R_L = 4Ω		99		dB
CS	Channel Separation	0dBr = 1W, R_L = 4Ω, f = 1 kHz	74	80		dB
PSRR	Power Supply Rejection Ratio	Vripple = 100mV	60	80		dB
η	Power Efficiency	P_{OUT} = 12W/Channel, R_L = 8Ω		88		%
V_{OFFSET}	Output Offset Voltage	No Load, MUTE = Logic low		50	150	mV
V_{OH}	High-level output voltage (FAULT & OVERLOADB)		3.5			V
V_{OL}	Low-level output voltage (FAULT & OVERLOADB)				1	V
e_{OUT}	Output Noise Voltage	A-Weighted, input AC grounded		100		μV

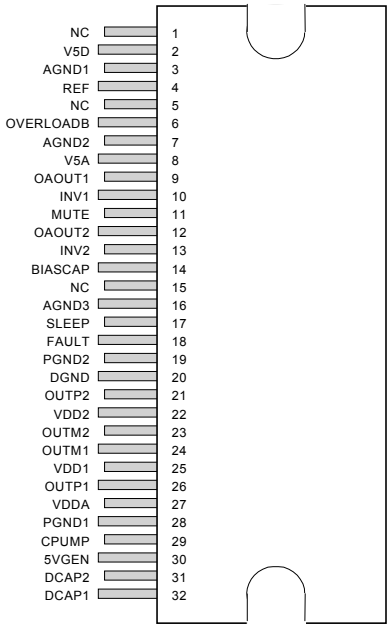
Note 6: Minimum and maximum limits are guaranteed but may not be 100% tested.
Note 7: For operation in ambient temperatures greater than 25°C, the device must be derated based on the maximum junction temperature and the thermal resistance determined by the mounting technique.

PIN DESCRIPTION

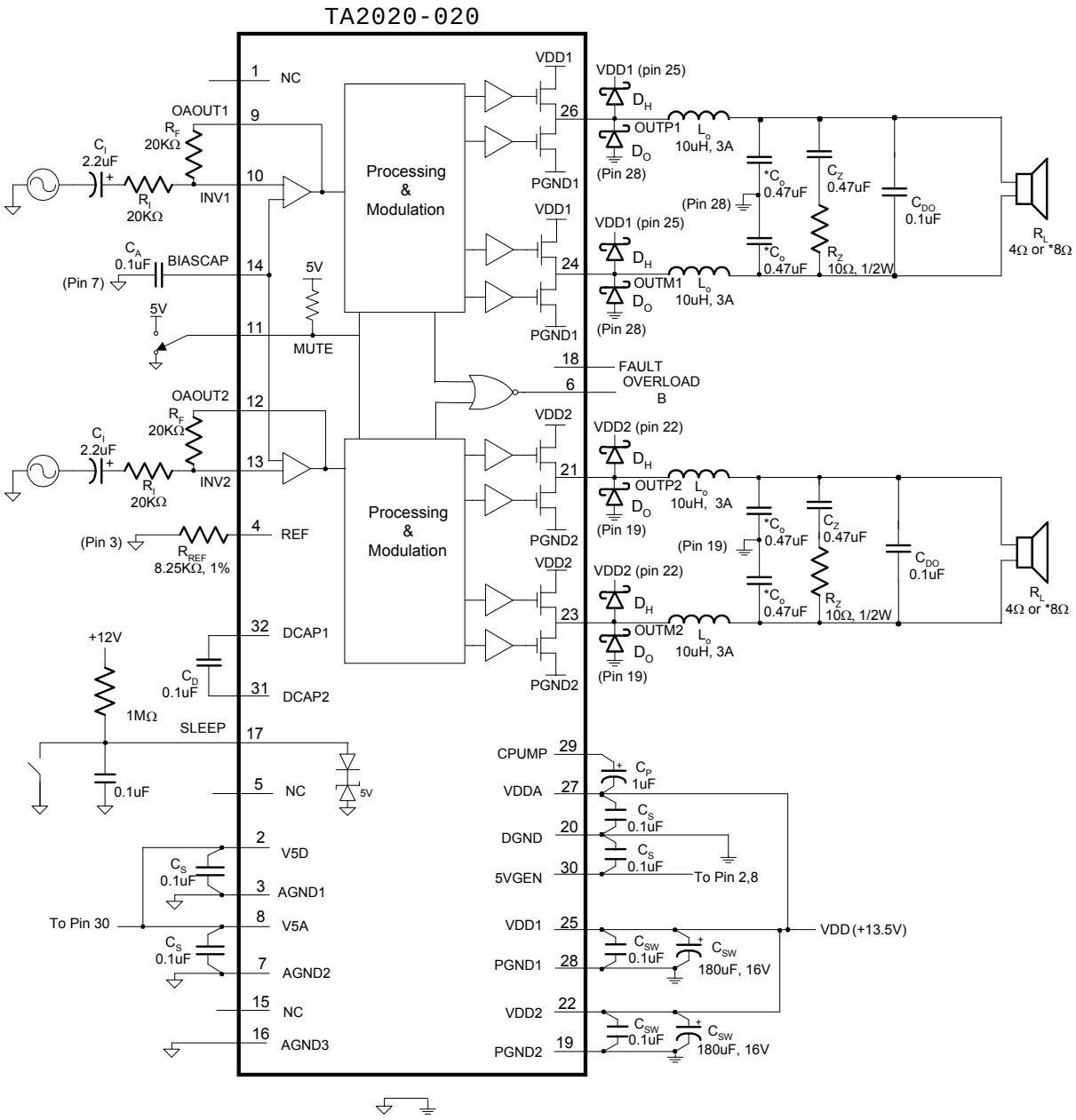
Pin	Function	Description
2, 8	V5D, V5A	Digital 5VDC, Analog 5VDC
3, 7, 16	AGND1, AGND2, AGND3	Analog Ground
4	REF	Internal reference voltage; approximately 1.0VDC
6	OVERLOADB	A logic low output indicates the input signal has overloaded the amplifier.
9, 12	OAOUT1, OAOUT2	Input stage output pins
10, 13	INV1, INV2	Single-ended inputs. Inputs are a "virtual" ground of an inverting opamp with approximately 2.4VDC bias.
11	MUTE	When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. Ground if not used.
14	BIASCAP	Input stage bias voltage (approximately 2.4VDC).
17	SLEEP	When set to logic high, device goes into low power mode. If not used this pin should be grounded. Can be pulled-up to V_{DD} with a 1MΩ resistor (100KΩ minimum).
18	FAULT	A logic high output indicates thermal overload, or an output is shorted to ground, or another output.
19, 28	PGND2, PGND1	Power Ground (high current)
20	DGND	Digital Ground. Should be connected to AGND locally at TA2020-020.
21, 23, 26, 24	OUTP2 & OUTM2; OUTP1 & OUTM1	Bridged output pairs
22, 25	VDD2, VDD1	Supply pin for high current H-bridges, nominally 13.5VDC.
1, 5, 15	NC	Not connected
27	VDDA	Analog 13.5VDC
29	CPUMP	Charge pump output (nominally 10V above VDDA)
30	5VGEN	Regulated 5VDC source used to supply power to the input section (pins 2 & 8).
31, 32	DCAP2, DCAP1	Charge pump switching pins. DCAP1 (pin 32) is a free running 300kHz square wave between VDDA and DGND (13.5Vpp nominal). DCAP2 (pin 31) is level shifted 10 volts above DCAP1 (pin 32) with the same amplitude (13.5Vpp nominal), frequency, and phase as DCAP1.

TA2020 PINOUT

32-pin SSIP Package
(Front View)



APPLICATION /TEST CIRCUIT



Note: Analog and Digital/Power Grounds must be connected locally at the TA2020-020

Analog Ground

Digital/Power Ground

Diodes (D_O and D_H) are Motorola MBRS130T3 (the D_H diodes are required for V_{DD}>13.5V)

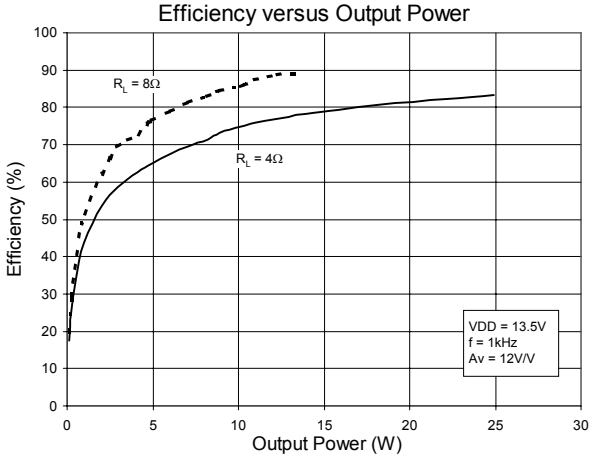
* Use C_o = 0.22µF and Cz=0.22uF for 8 Ohm loads

EXTERNAL COMPONENTS DESCRIPTION (Refer to the Application/Test Circuit)

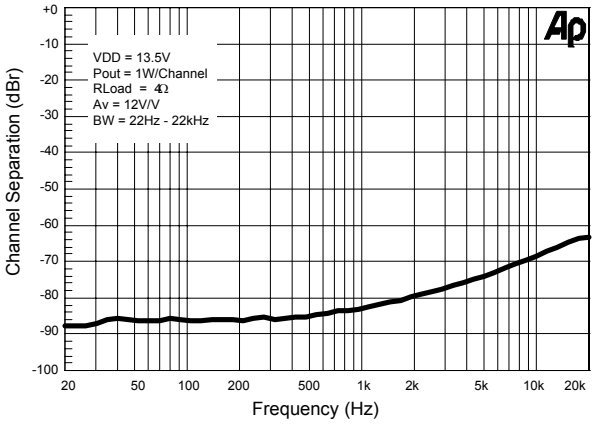
Components	Description
R_I	Inverting input resistance to provide AC gain in conjunction with R_F. This input is biased at the BIASCAP voltage (approximately 2.4VDC).
R_F	Feedback resistor to set AC gain in conjunction with R_I $A_V = 12(R_F / R_I)$. Please refer to the Amplifier Gain paragraph, in the Application Information section.
C_I	AC input coupling capacitor which, in conjunction with R_I, forms a highpass filter at $f_C = 1/(2\pi R_I C_I)$.
R_{REF}	Bias resistor. Locate close to pin 4 and ground at pin 7.
C_A	BIASCAP decoupling capacitor. Should be located close to pin 14 and grounded at pin 7.
C_D	Charge pump input capacitor. This capacitor should be connected directly between pins 31 and 32 and located physically close to the TA2020-020.
C_P	Charge pump output capacitor that enables efficient high side gate drive for the internal H-bridges. To maximize performance, this capacitor should be connected directly between pin 29 (CPUMP) and pin 27 (VDDA). Please observe the polarity shown in the Application/Test Circuit.
C_S	Supply decoupling for the low current power supply pins. For optimum performance, these components should be located close to the pin and returned to their respective ground as shown in the Application/Test Circuit.
C_{SW}	Supply decoupling for the high current H-Bridge supply pins. These components must be located as close to the device as possible to minimize supply overshoot and maximize device reliability. Both the high frequency bypassing (0.1uF) and bulk capacitor (180uF) should have good high frequency performance including low ESR and low ESL. Panasonic HFQ or FC capacitors are ideal for the bulk capacitor.
C_Z	Zobel capacitor, which in conjunction with R_Z, terminates the output filter at high frequencies
R_Z	Zobel resistor, which in conjunction with C_Z, terminates the output filter at high frequencies. The combination of R_Z and C_Z minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with increasing frequency. Depending on the program material, the power rating of R_Z may need to be adjusted. The typical value is ½ watt.
D_O	Schottky diodes that minimize undershoots of the outputs with respect to power ground during switching transitions. For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective PGND. Please see Application/Test Circuit for ground return pin.
D_H	Schottky diodes that minimize overshoots of the outputs with respect to V_{DD} during switching transitions (required for applications where V_{DD} >13.5V). For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective V_{DD} pins. Please see Application/Test Circuit for V_{DD} return pin.
L_O	Output inductor, which in conjunction with C_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$.
C_O	Output capacitor which in conjunction with L_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order low-pass filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$.
C_{DO}	Differential output capacitor.

TYPICAL PERFORMANCE

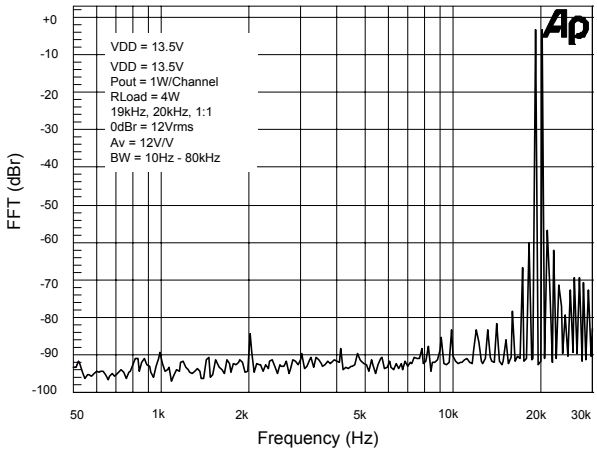
Efficiency versus Output Power



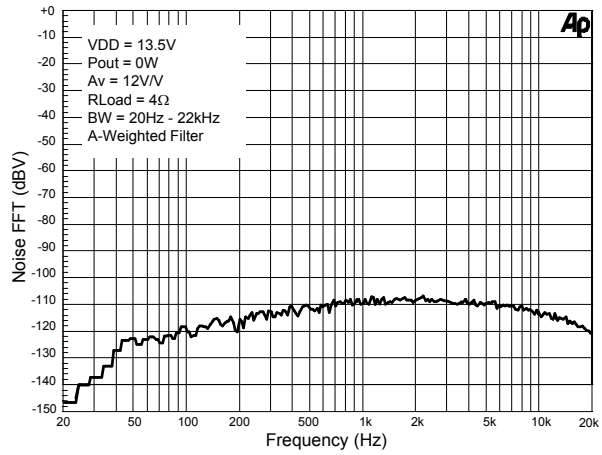
Channel Separation versus Frequency



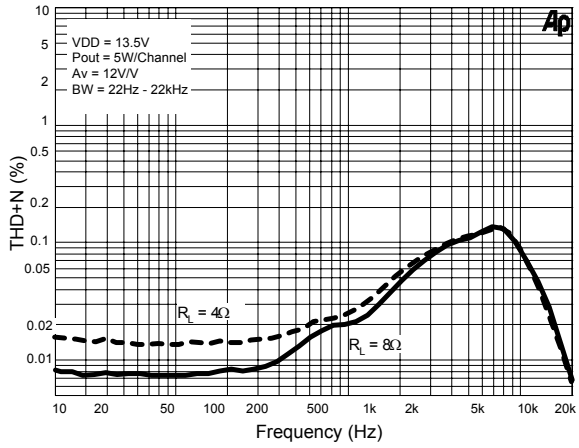
Intermodulation Performance



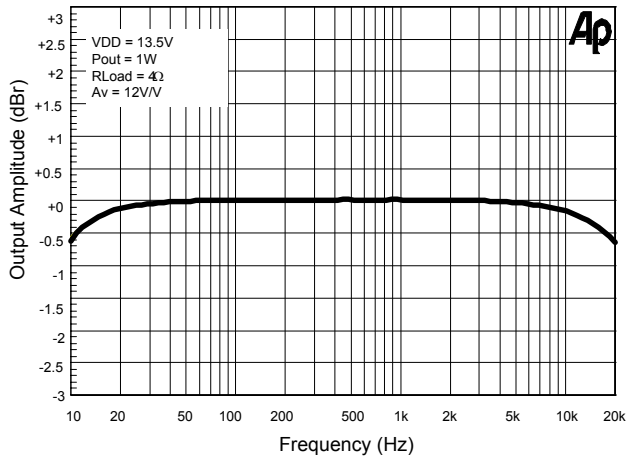
Noise Floor



THD+N versus Frequency



Frequency Response

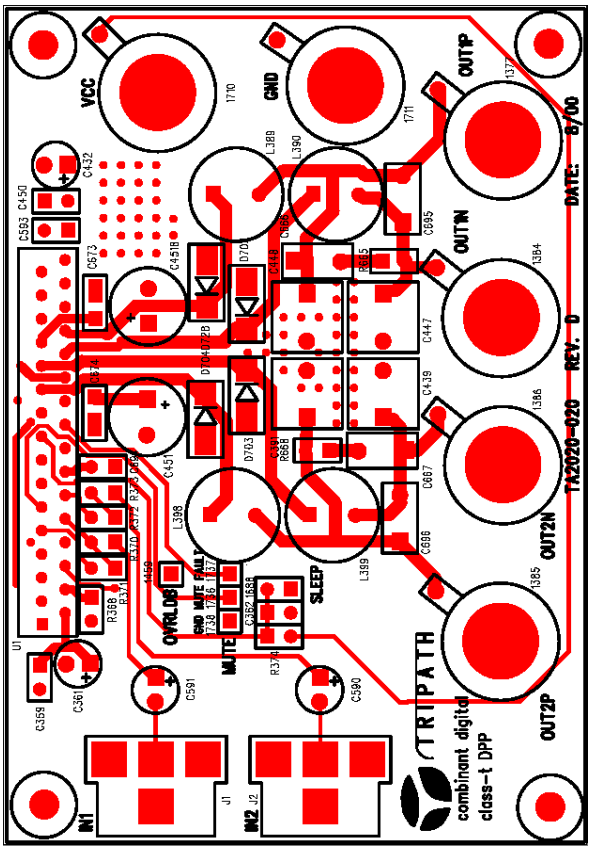


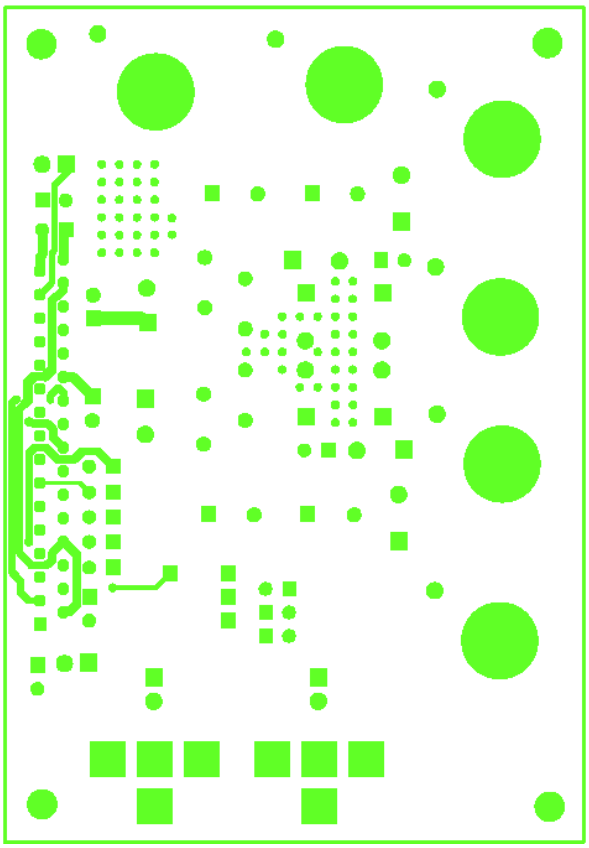
APPLICATION INFORMATION

Circuit Board Layout

The TA2020-020 is a power (high current) amplifier that operates at relatively high switching frequencies. The outputs of the amplifier switch between the supply voltage and ground at high speeds while driving high currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. To avoid subjecting the TA2020-020 to potentially damaging voltage stress, it is critical to have a good printed circuit board layout. It is recommended that Tripath's layout and application circuit be used for all applications and only be deviated from after careful analysis of the effects of any changes.

The figures below are the Tripath TA2020-020 evaluation board. Some of the most critical components on the board are the power supply decoupling capacitors. C674 and C451 must be placed right next to pins 22 and 19 as shown. C673 and C451B must be placed right next to pins 25 and 28 as shown. These power supply decoupling capacitors from the output stage not only help reject power supply noise, but they also absorb voltage spikes on the VDD pins caused by overshoots of the outputs of the amplifiers. Voltage overshoots can also be caused by output inductor flyback during high current switching events such as shorted outputs or driving low impedances at high levels. If these capacitors are not close enough to the pins, electrical overstress to the part can occur, possibly resulting in permanent damage to the TA2020-020.





TA2020 Amplifier Gain

The gain of the TA2020-020 is set by the ratio of two external resistors, R_I and R_F, and is given by the following formula:

$$\frac{V_O}{V_I} = -12\,\frac{R_F}{R_I}$$

where V_I is the input signal level and V_O is the differential output signal level across the speaker. Please note that OUTP1 and OUTP2 are 180° out of phase with their corresponding input signals.

20 watts of RMS output power results from an 8.944 V RMS signal across a four-ohm speaker load. If $R_F = R_I$, then 20 Watts will be achieved with 0.745 V RMS of input signal.

$$8.944\,V_{RMS} = \sqrt{(R_L * P_O)} = \sqrt{(4\Omega * 20W)}$$

Protection Circuits

The TA2020-020 is guarded against over-temperature and over-current conditions. When the device goes into an over-temperature or over-current state, the FAULT pin goes to a logic HIGH state indicating a fault condition. When this occurs, the amplifier is muted, all outputs are TRI-STATED, and will float to 1/2 of V_{DD}.

Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the part exceeds approximately 155°C. The thermal hysteresis of the part is approximately 45°C, therefore the fault will automatically clear when the junction temperature drops below 110°C.

Over-current Protection

An over-current fault occurs if more than approximately 7 amps of current flows from any of the amplifier output pins. This can occur if the speaker wires are shorted together or if one side of the speaker is shorted to ground. An over-current fault sets an internal latch that can only be cleared if the MUTE pin is toggled or if the part is powered down. Alternately, if the MUTE pin is connected to the FAULT pin, the HIGH output of the FAULT pin will toggle the MUTE pin and automatically reset the fault condition.

Overload

The OVERLOADB pin is a 5V logic output. When low, it indicates that the level of the input signal has overloaded the amplifier resulting in increased distortion at the output. The OVERLOADB signal can be used to control a distortion indicator light or LED through a simple buffer circuit.

Sleep Pin

The SLEEP pin is a 5V logic input that when pulled high (>3.5V) puts the part into a low quiescent current mode. This pin is internally clamped by a zener diode to approximately 6V thus allowing the pin to be pulled up through a large valued resistor (1MΩ recommended, 100KΩ minimum) to V_{DD}. To disable SLEEP mode, the sleep pin should be grounded

Fault Pin

The FAULT pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: low supply voltage, low charge pump voltage, low 5V regulator voltage, over current at any output, and junction temperature greater than approximately 155°C. The FAULT output is capable of directly driving an LED through a series 2KΩ resistor. If the FAULT pin is connected directly to the MUTE input an automatic reset will occur in the event of an over-current condition.

Heat Sink Requirements

In some applications it may be necessary to fasten the TA2020-020 to a heat sink. The determining factor is that the 150°C maximum junction temperature, T_J(max) cannot be exceeded, as specified by the following equation:

$$P_{DISS} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}}$$

where…
P_{DISS} = maximum power dissipation
T_{JMAX} = maximum junction temperature of TA2020-020
T_A = operating ambient temperature
θ_{JC} = junction-to-case thermal resistance of TA2020-020

Example:

What size heat sink is required to operate the TA2020-020 at 20W per channel into a 4Ω load continuously in a 70ºC ambient temperature?

P_{DISS} is determined by:

$$\text{Efficiency} = \eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} - P_{DISS}}$$

$$P_{DISS}\ (\text{per channel}) = \frac{P_{OUT}}{\eta} - P_{OUT} = \frac{20}{0.8} - 20 = 5\text{W}$$

Thus, P_{DISS} for two channels = 10W

$$\theta_{JA} = \frac{\left(T_{J(MAX)} - T_A\right)}{P_{DISS}} = \frac{150 - 70}{10} = 8°\text{C/W}$$

The θ_{JA} of the TA2020-020 in free air is 15°C/W. The θ_{JC} of the TA2020-020 is 3.5°C/W, so a heat sink of 4.5°C/W is required for this example. In actual applications, other factors such as the average P_{DISS} with a music source (as opposed to a continuous sine wave) and regulatory agency testing requirements will determine the size of the heat sink required.

Performance Measurements of the TA2020-020

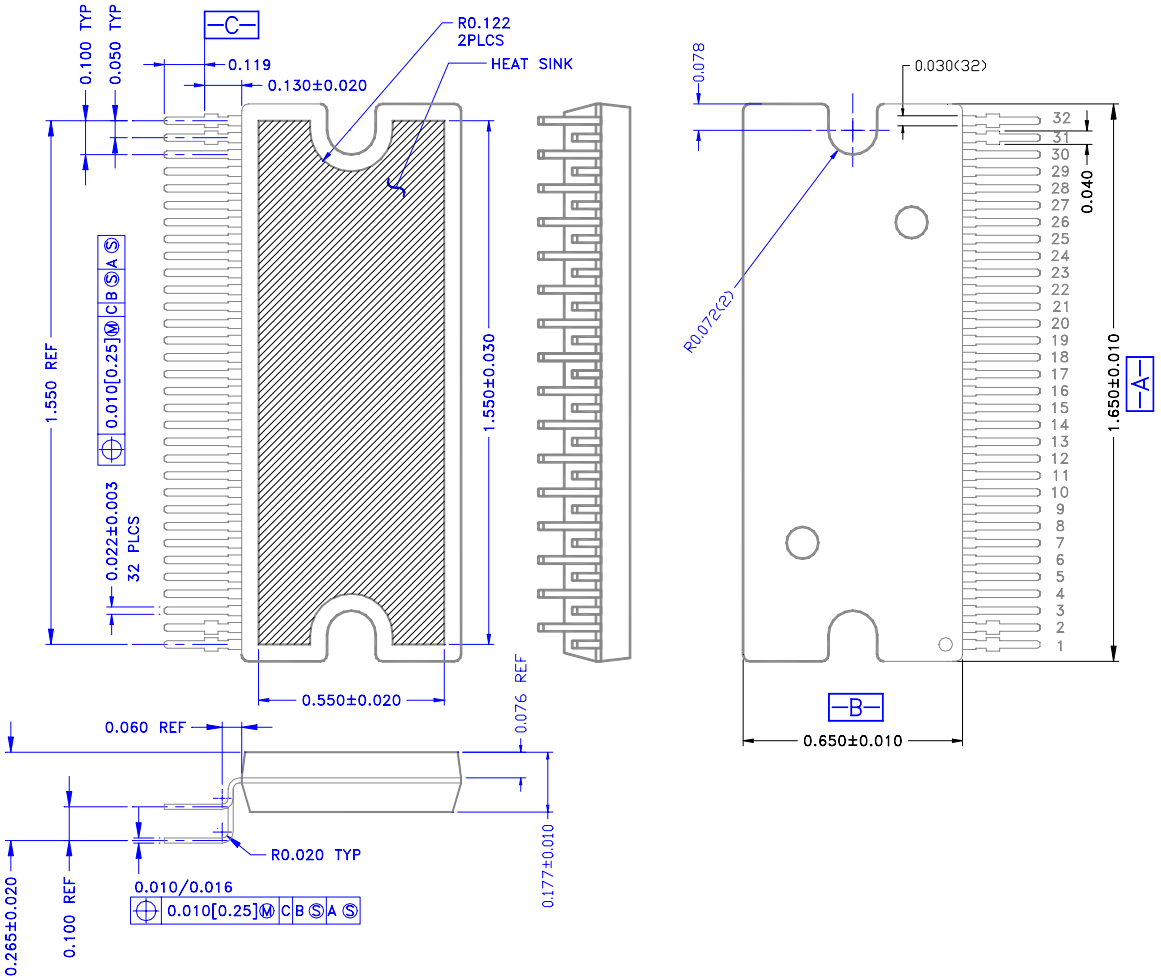
The TA2020-020 operates by generating a high frequency switching signal based on the audio input. This signal is sent through a low-pass filter (external to the Tripath amplifier) that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum in nature and typically varies between 100kHz and 1MHz, which is well above the 20Hz – 20kHz audio band. The pattern itself does not alter or distort the audio input signal, but it does introduce some inaudible components.

The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the TA2020-020 amplifier switching pattern will degrade the measurement.

One feature of the TA2020-020 is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TA2020-020 Evaluation Board uses the Application/Test Circuit of this data sheet, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

PACKAGE INFORMATION

32-pin SSIP Package



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